



1/46

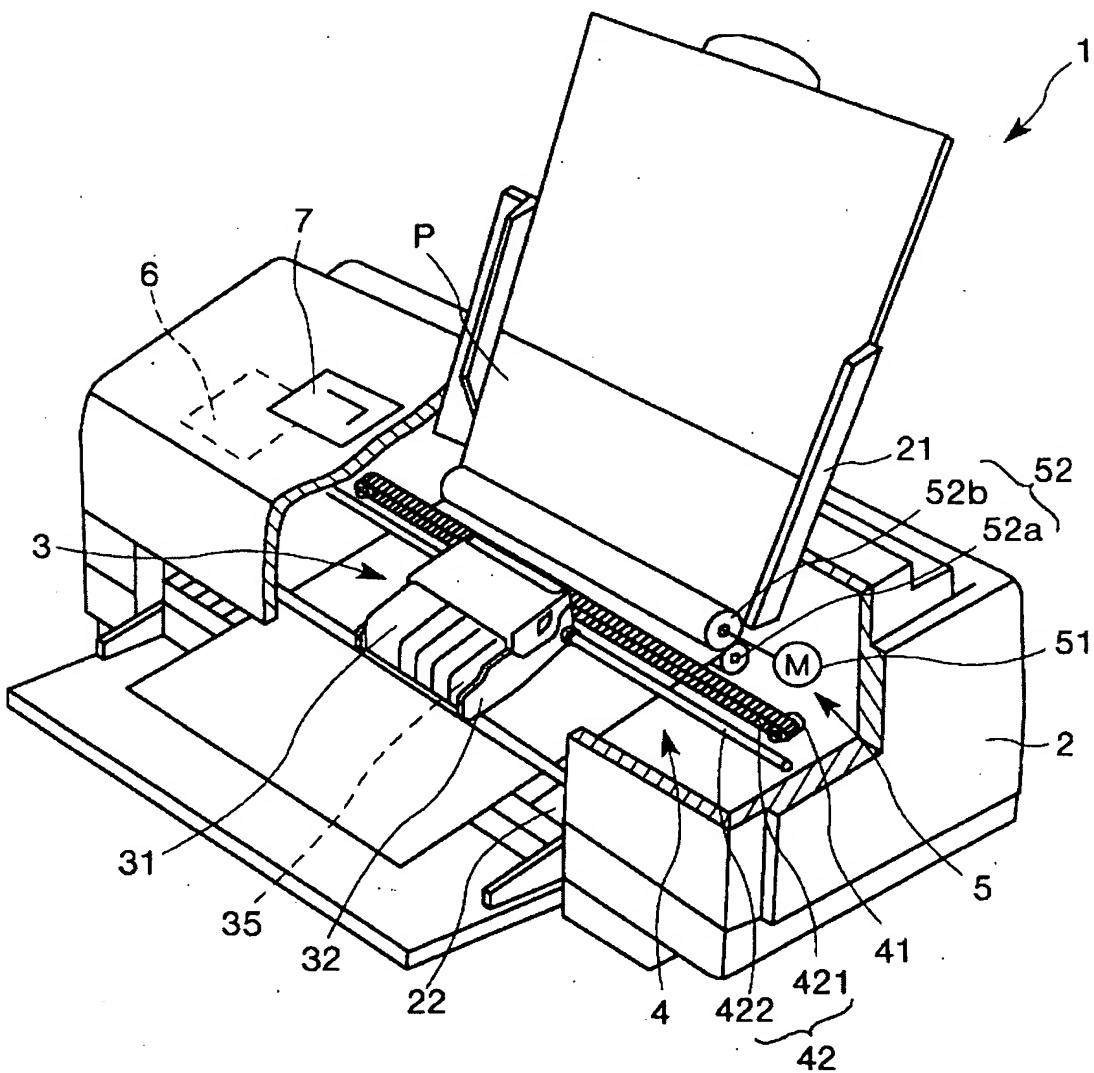


Fig. 1

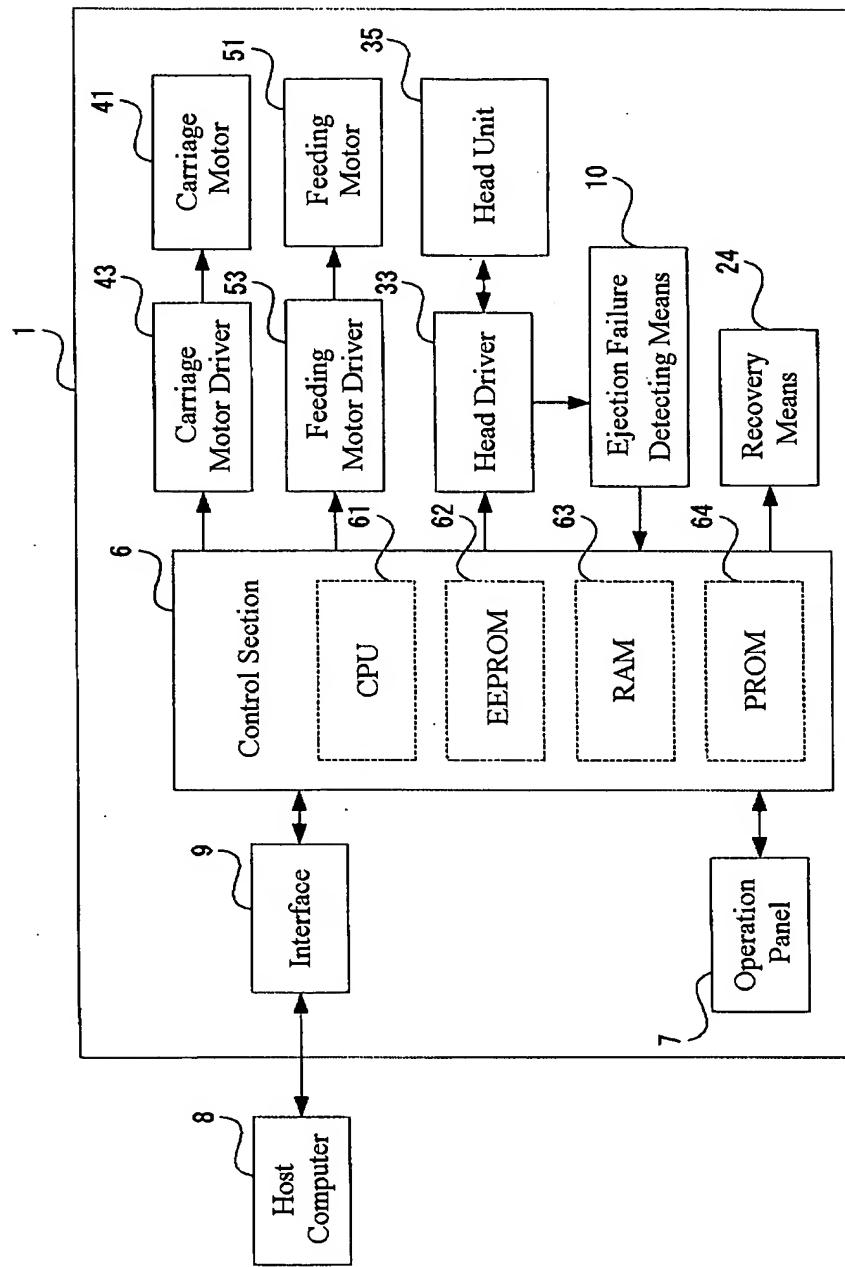


Fig. 2

3/46

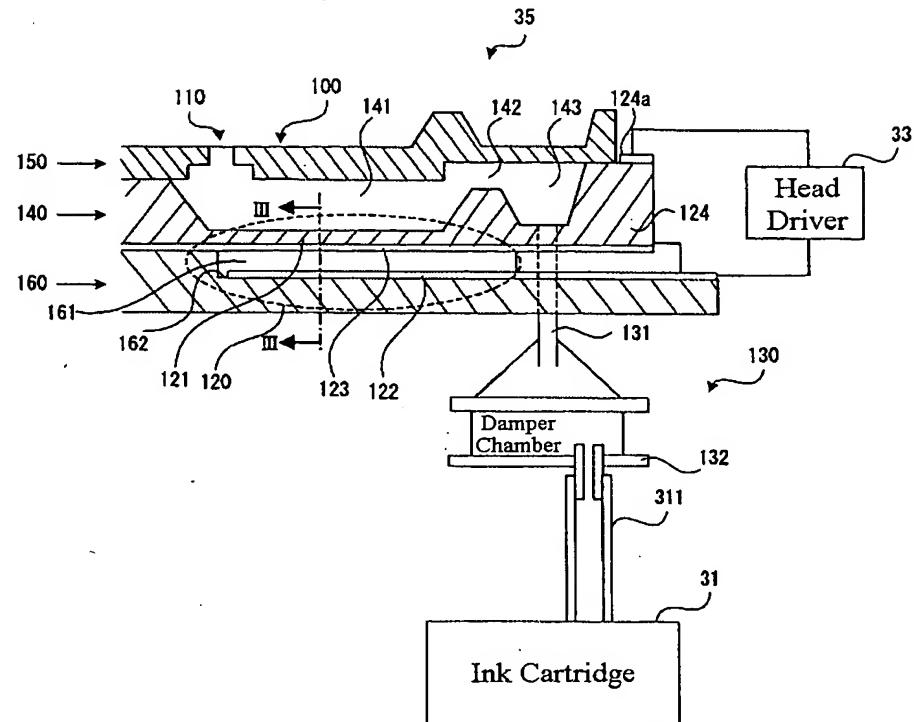


Fig. 3

4/46

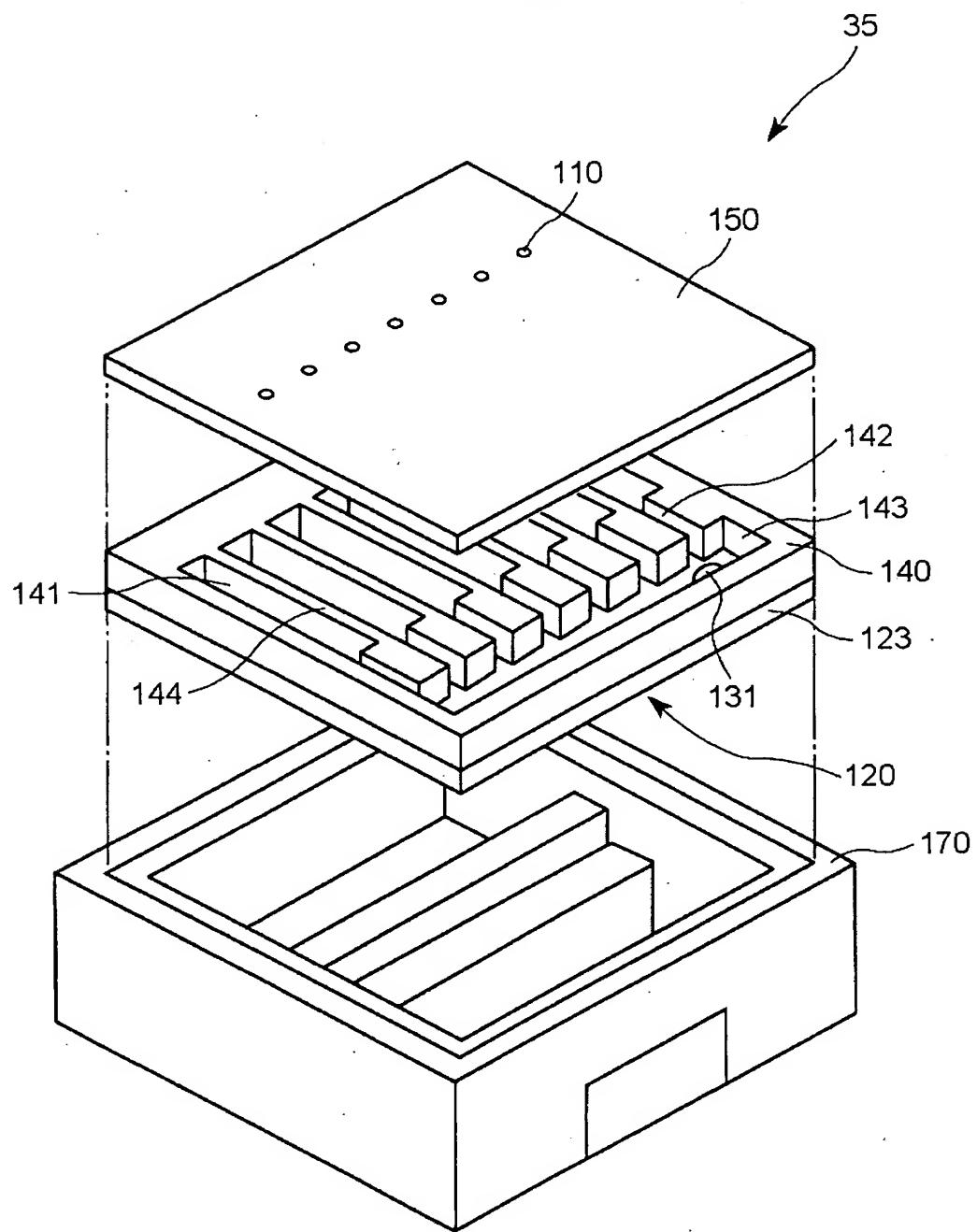


Fig. 4

5/46

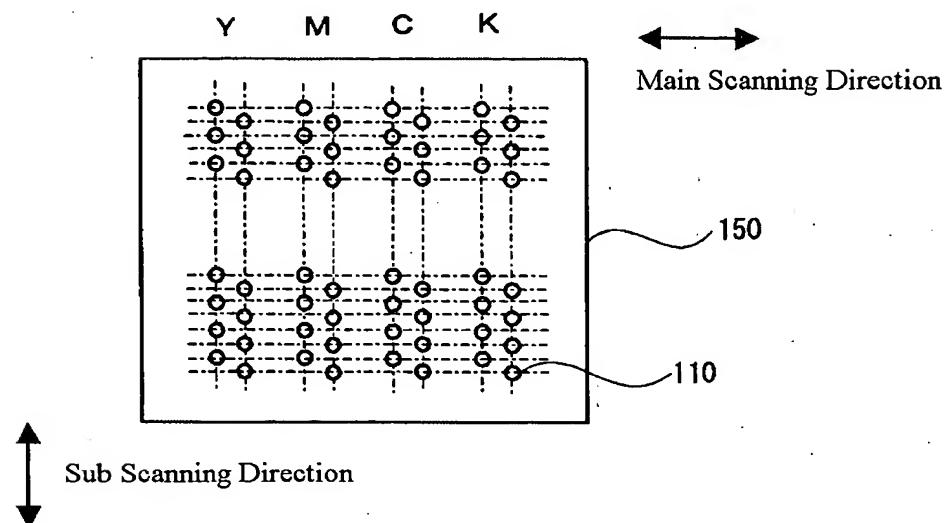


Fig. 5

6/46

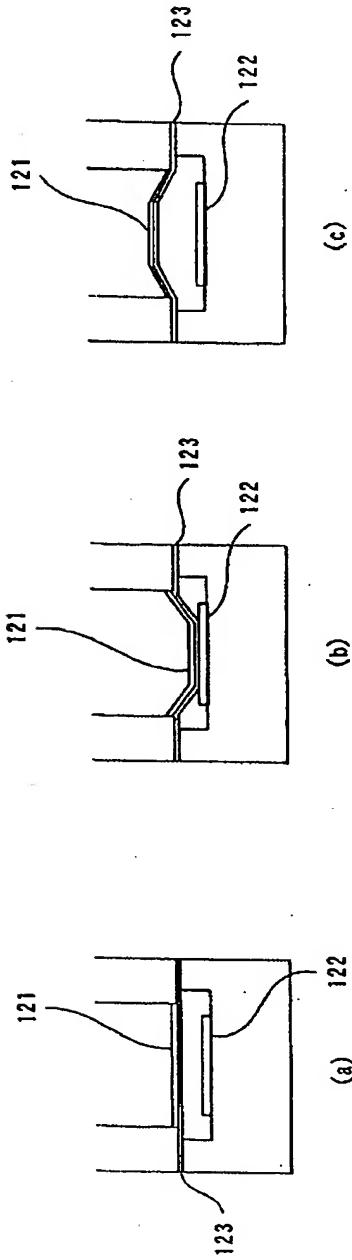


Fig. 6

7/46

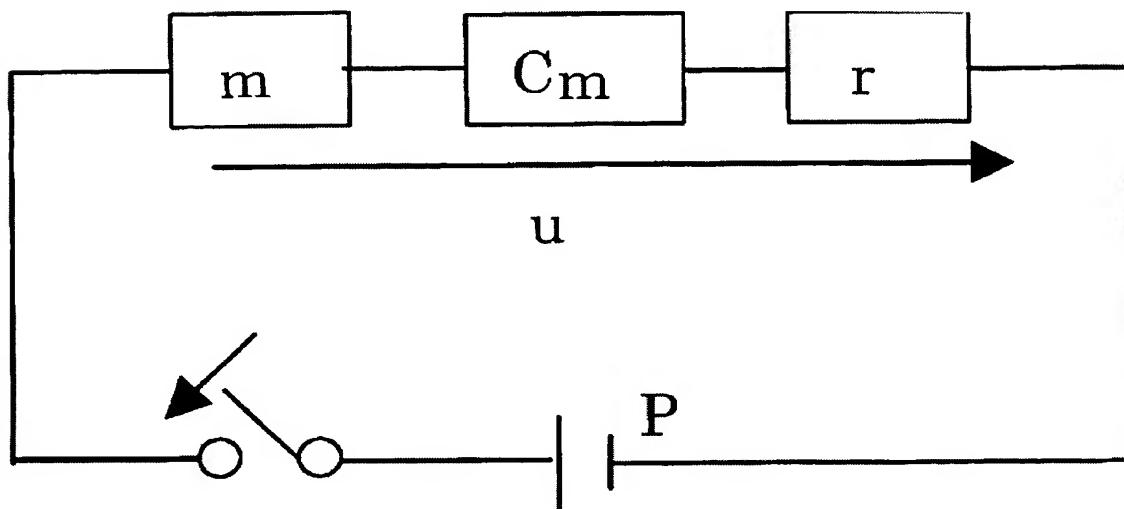


Fig. 7

8/46

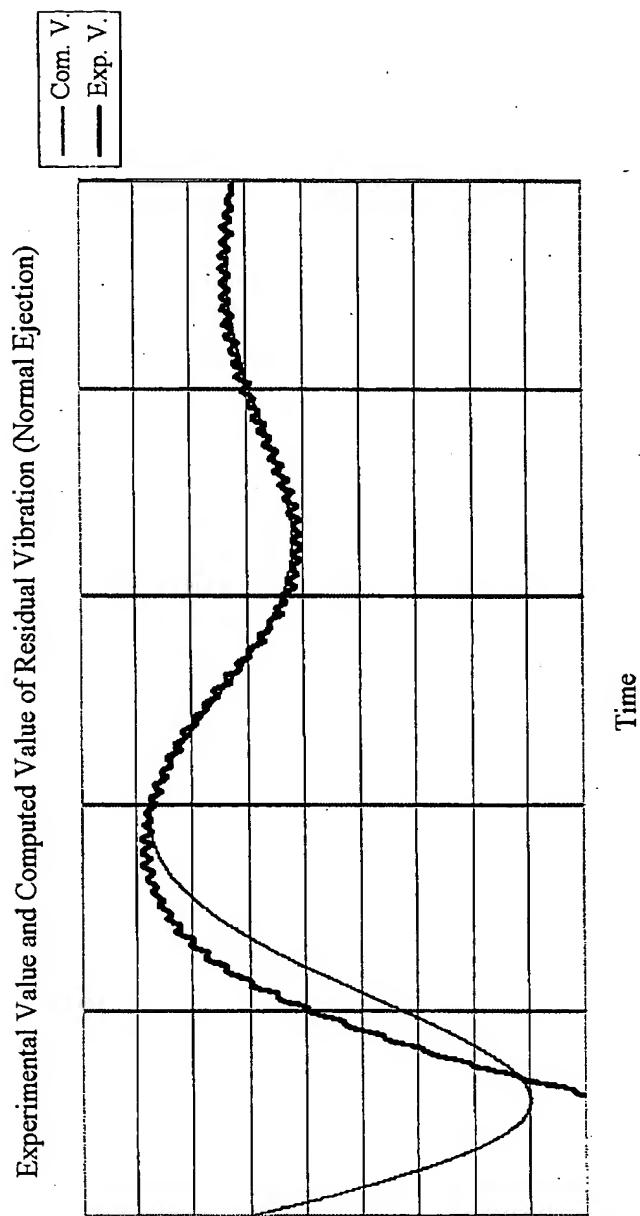


Fig. 8

9/46

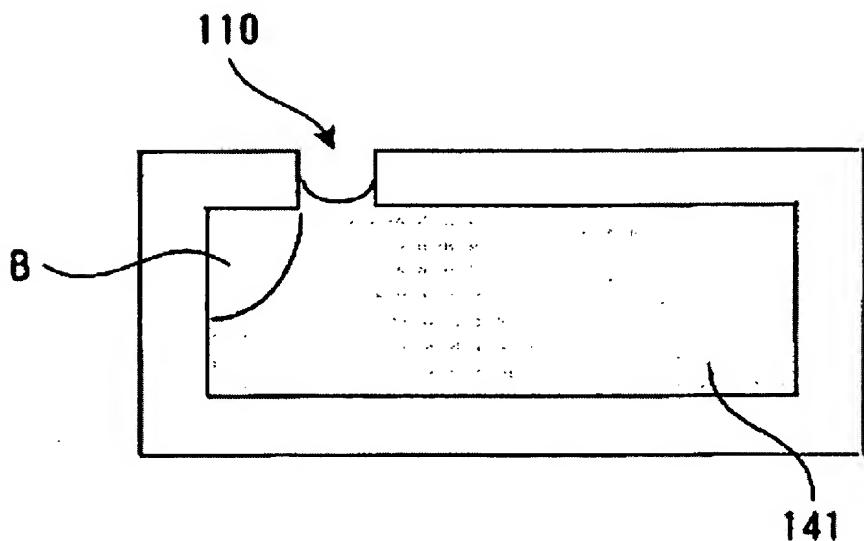


Fig. 9

10/46

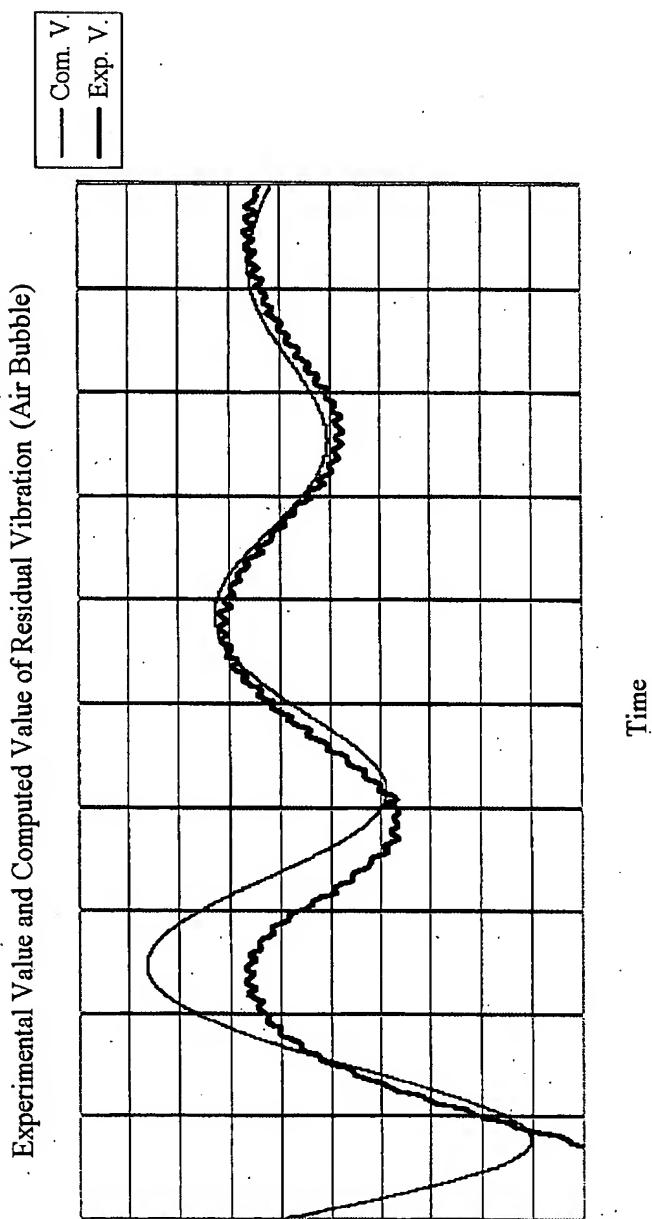


Fig. 10

11/46

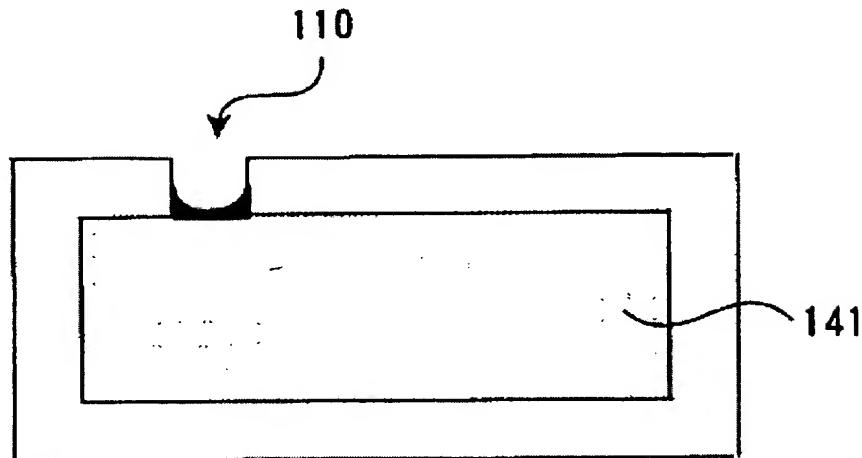


Fig. 11

12/46

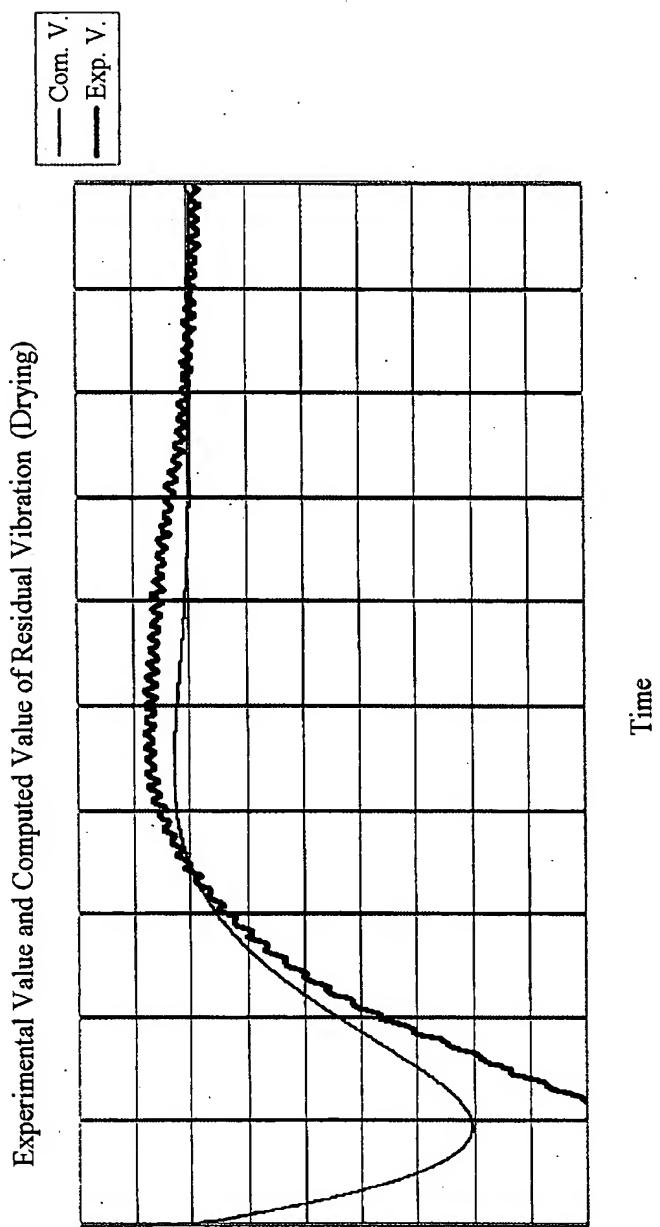


Fig. 12

13/46

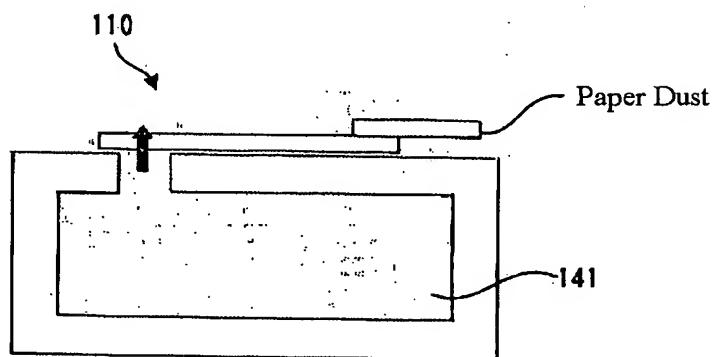


Fig. 13

14/46

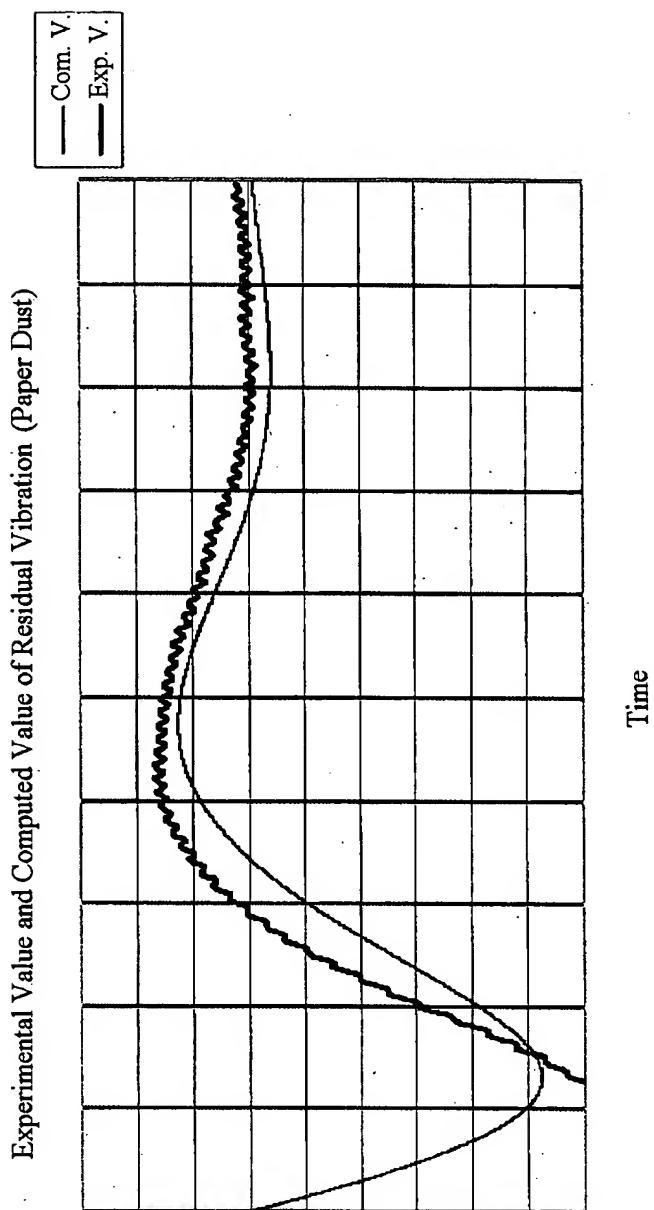


Fig. 14

15/46

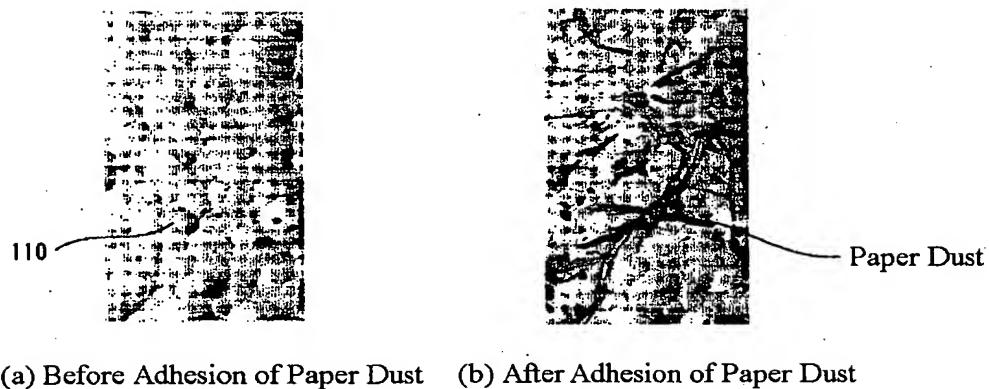


Fig. 15

16/46

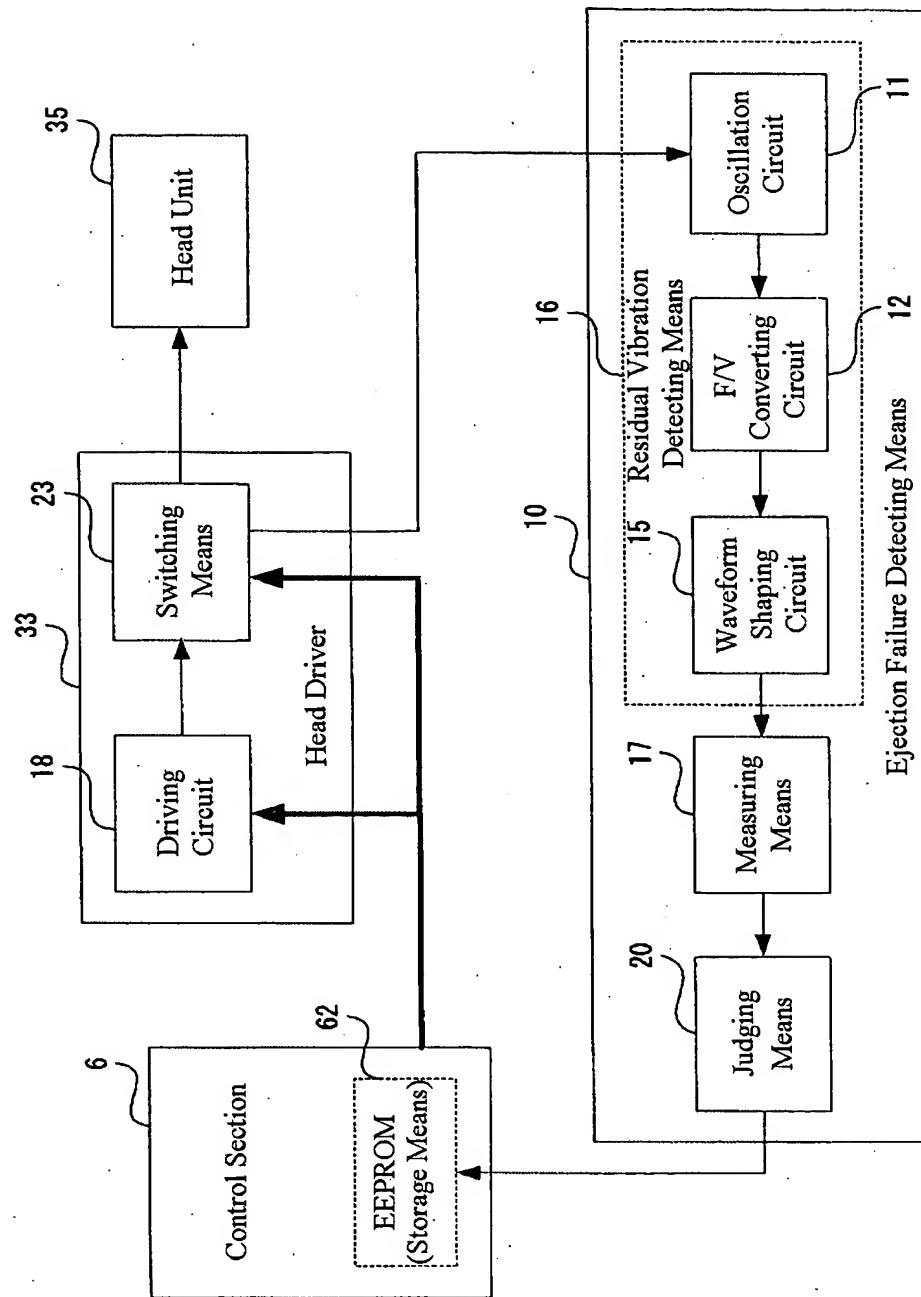


Fig. 16

17/46

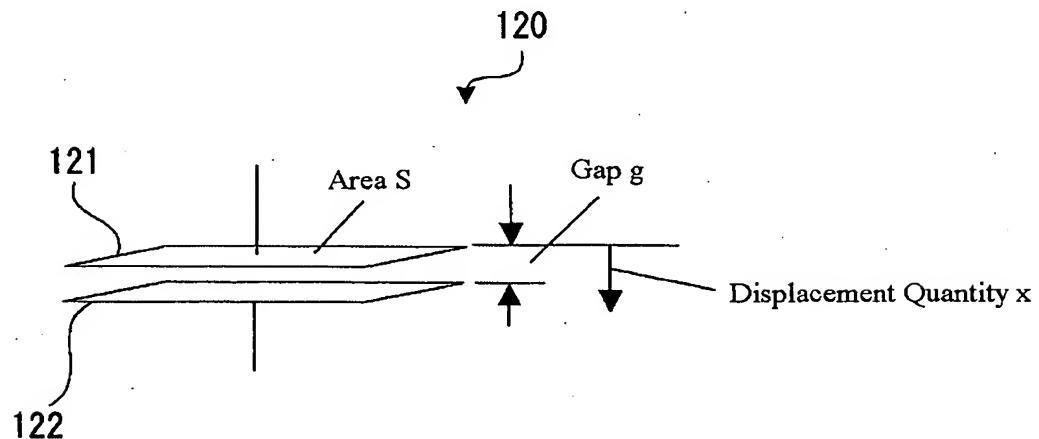


Fig. 17

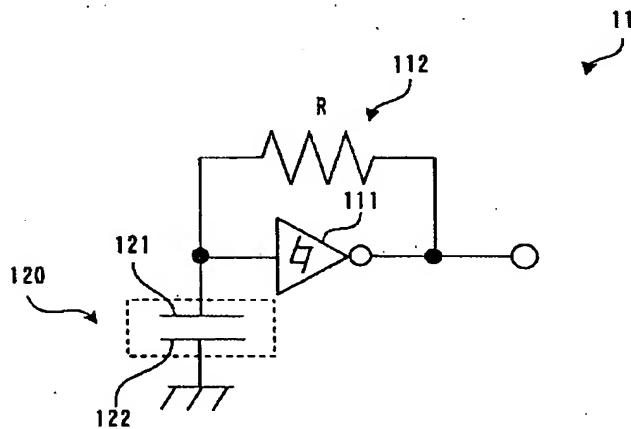


Fig. 18

18/46

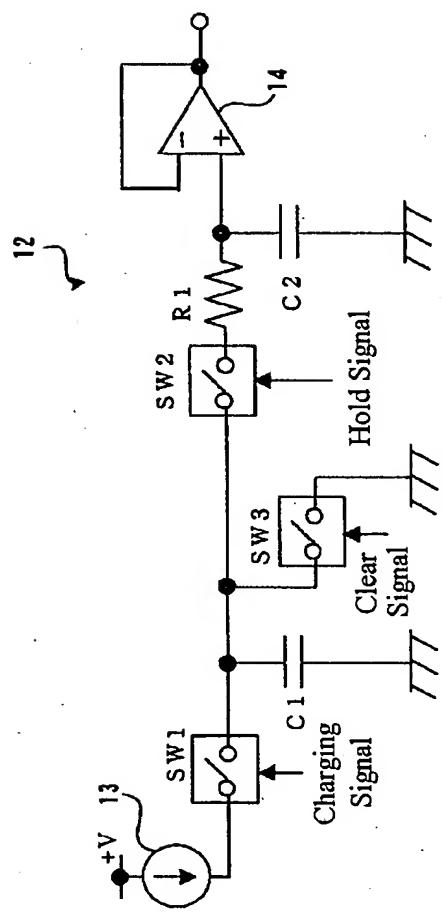


Fig. 19

19/46

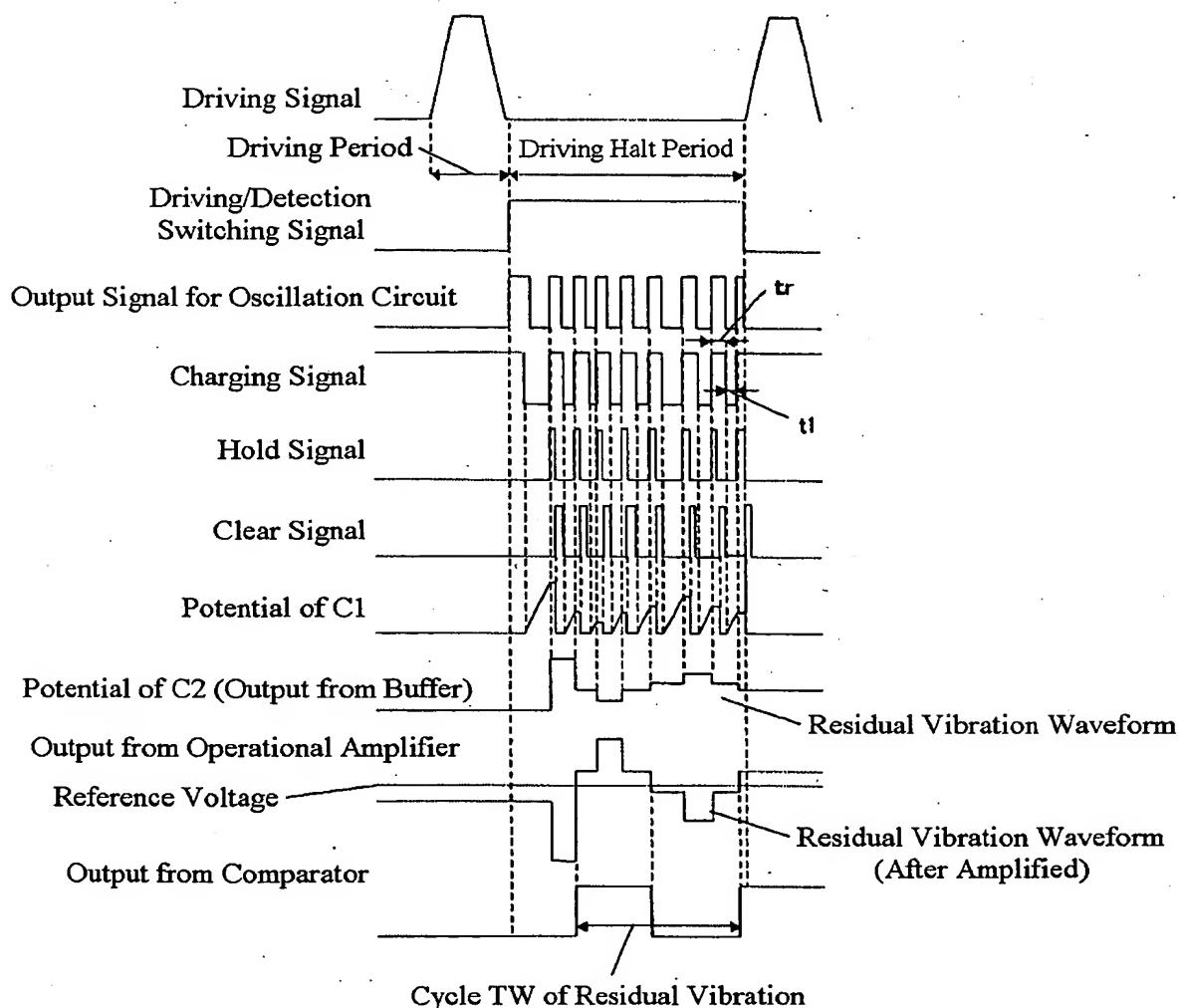


Fig. 20

20/46

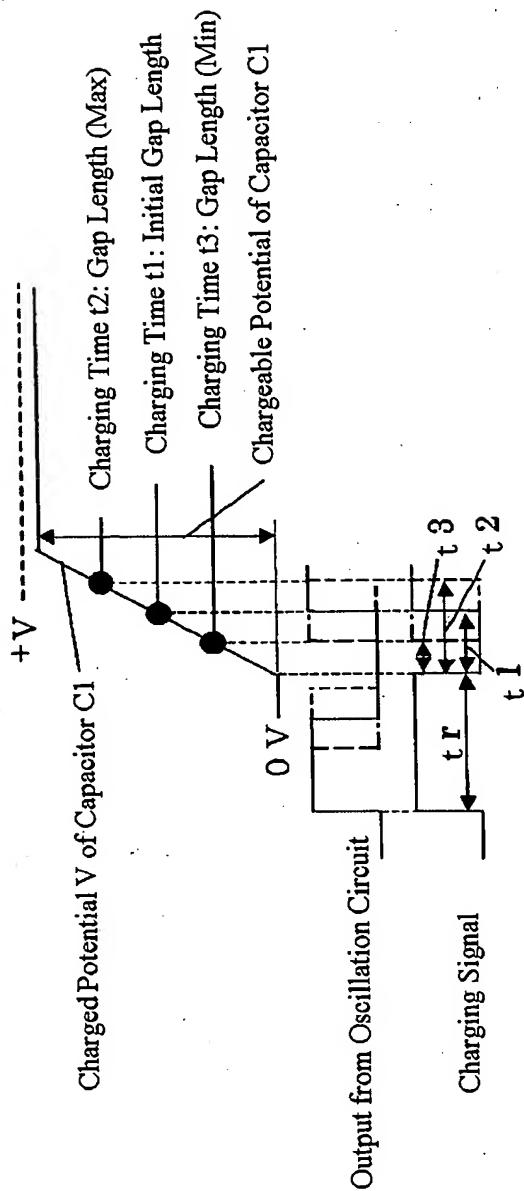


Fig. 21

21/46

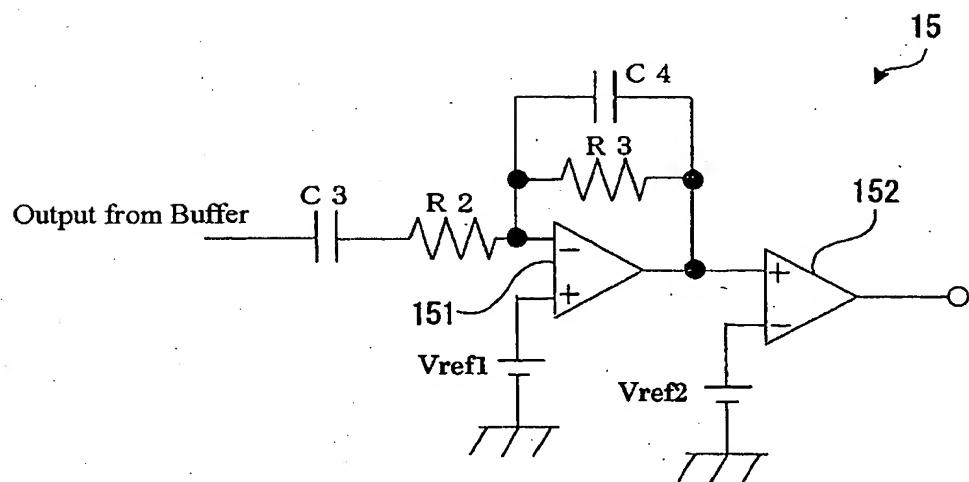


Fig. 22

22/46

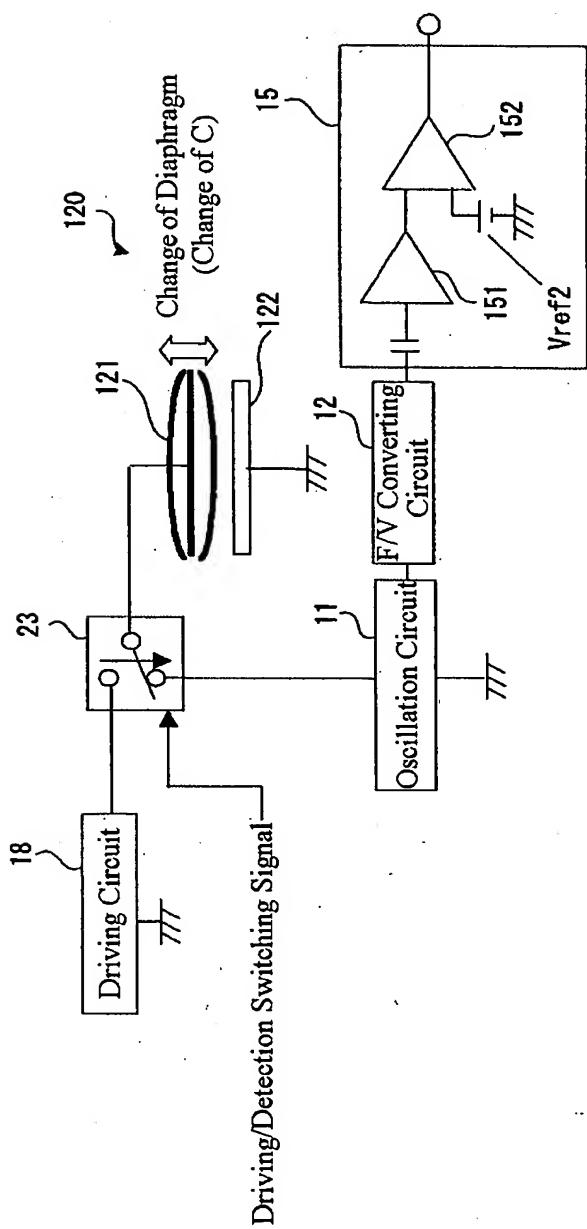


Fig. 23

23/46

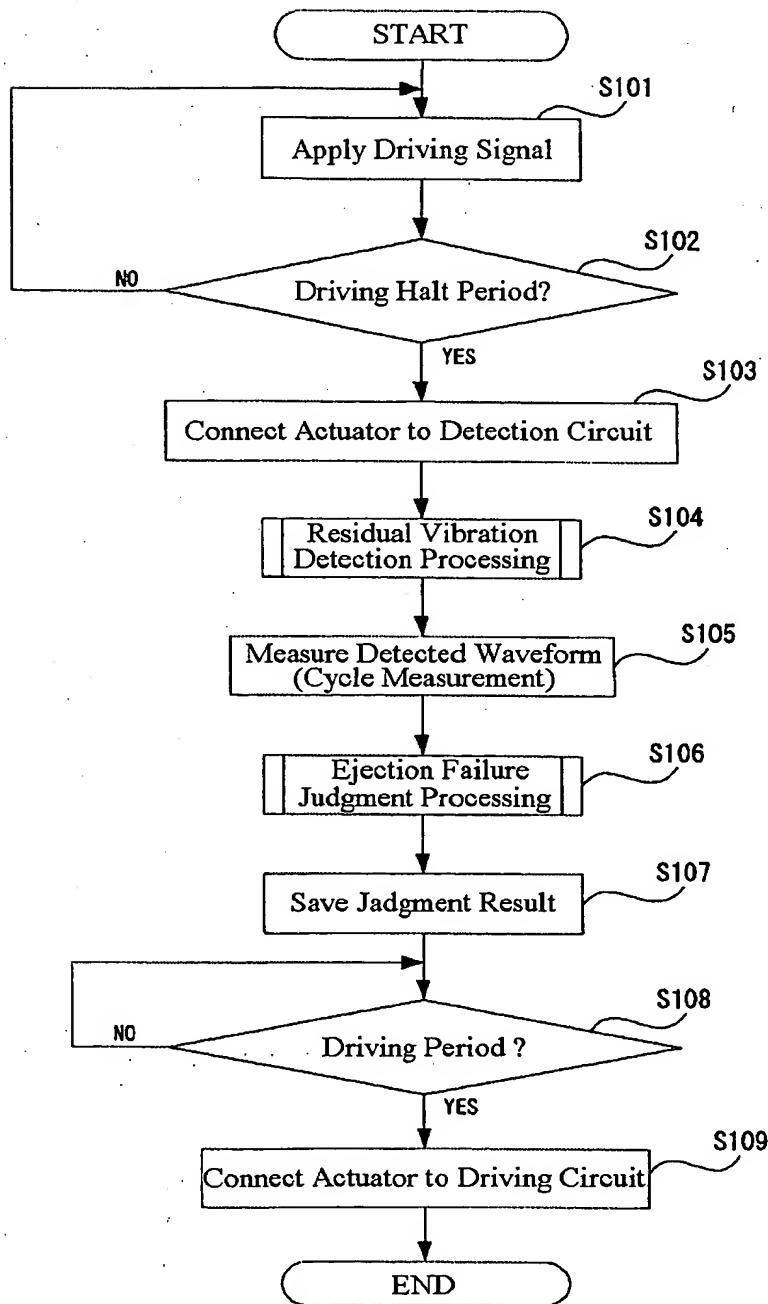


Fig. 24

24/46

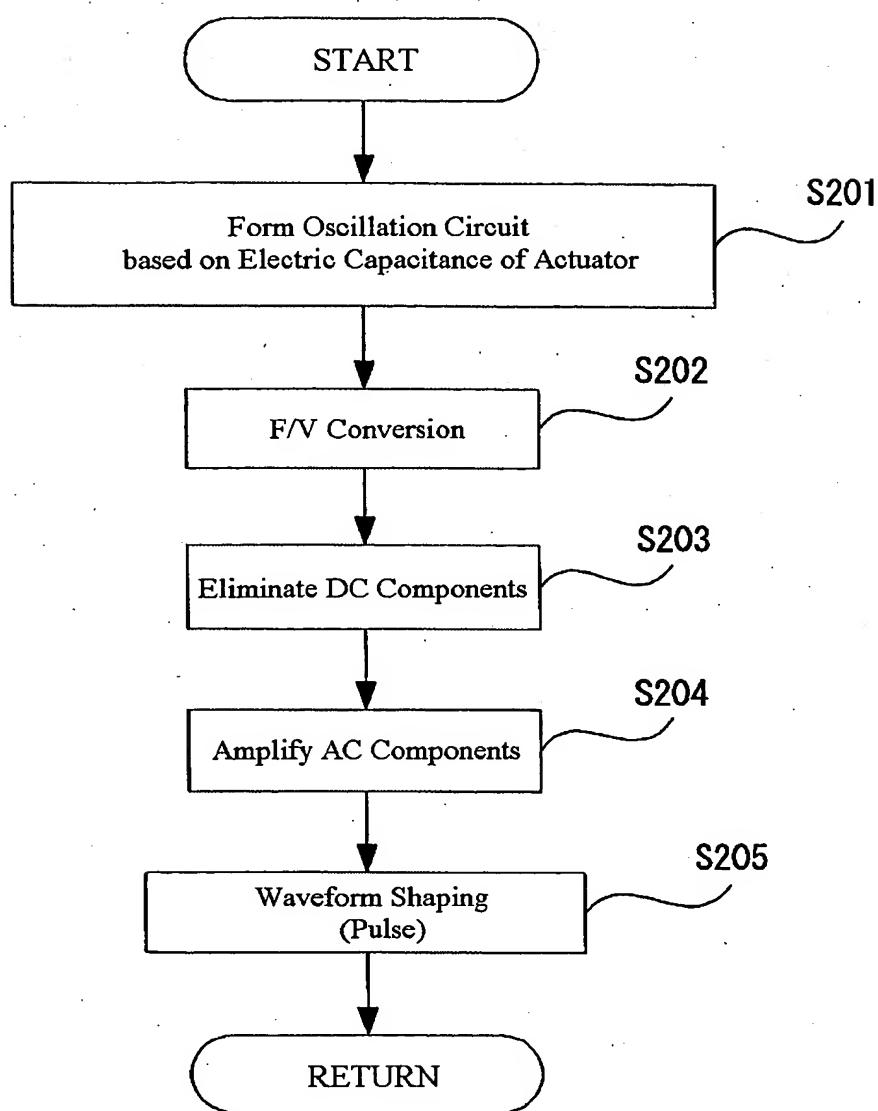


Fig. 25

25/46

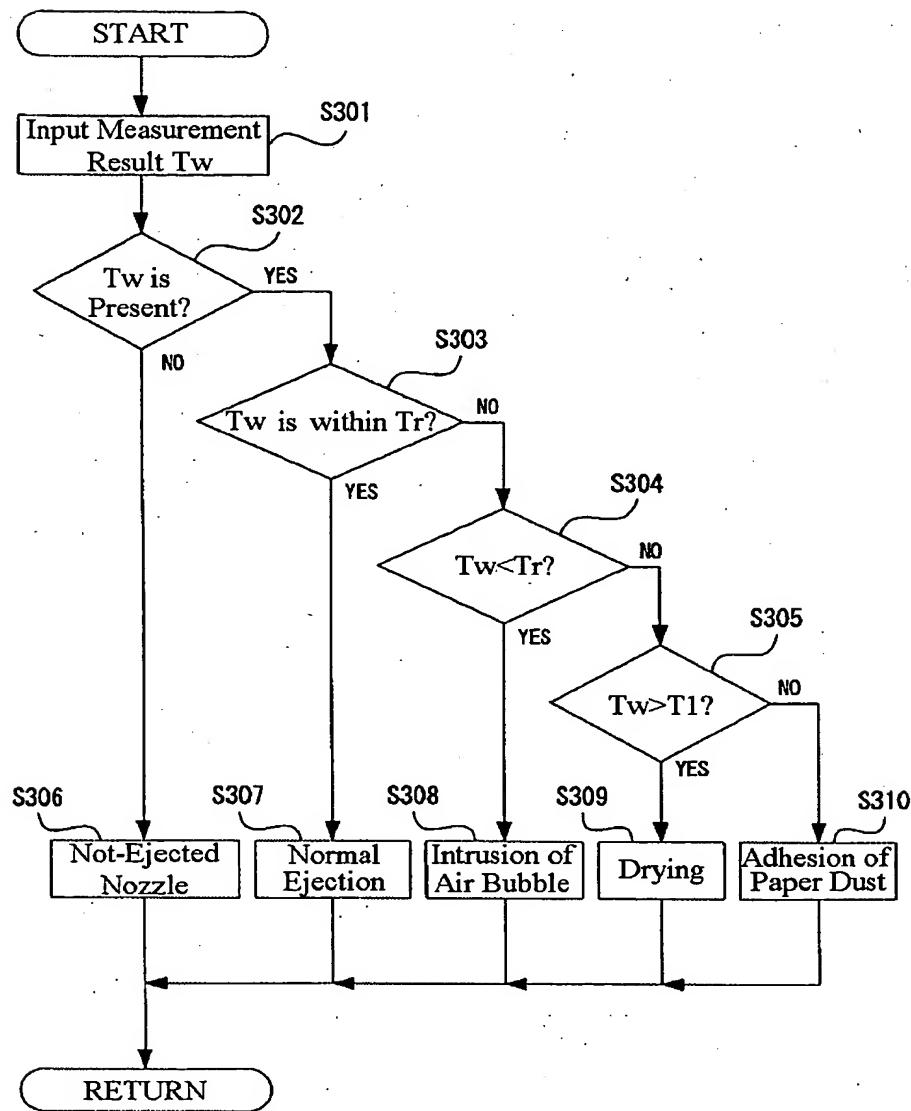


Fig. 26

26/46

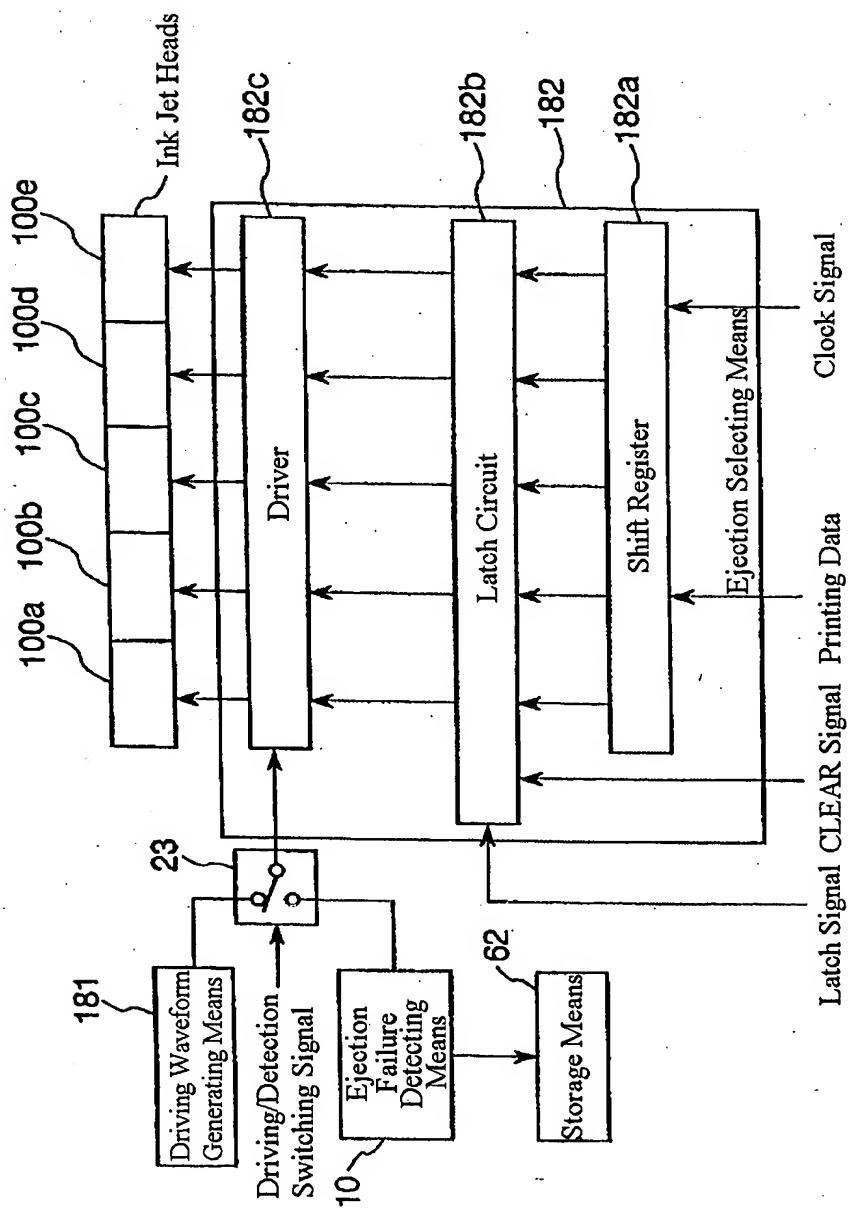
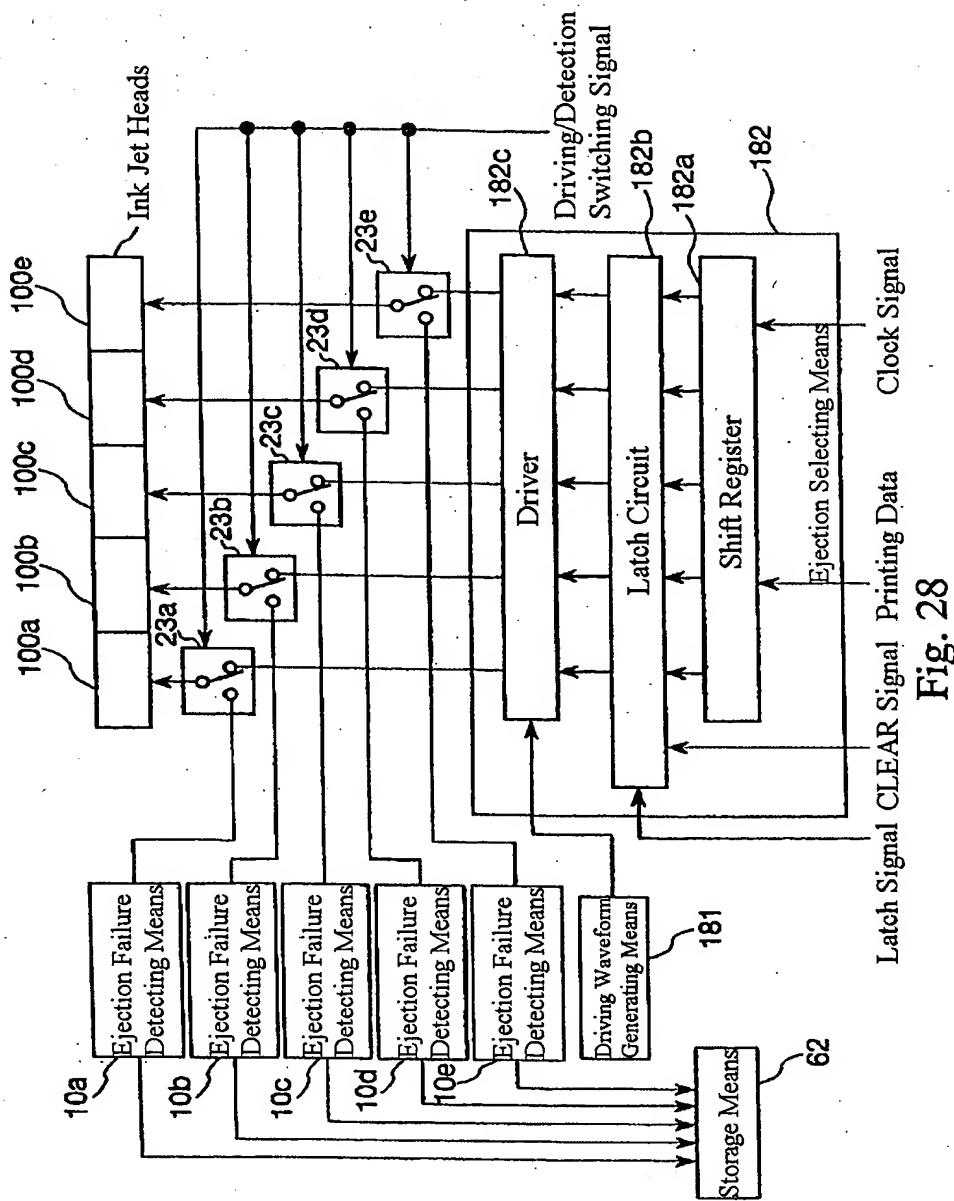


Fig. 27

27/46



Latch Signal CLEAR Signal Printing Data Clock Signal

Fig. 28

28/46

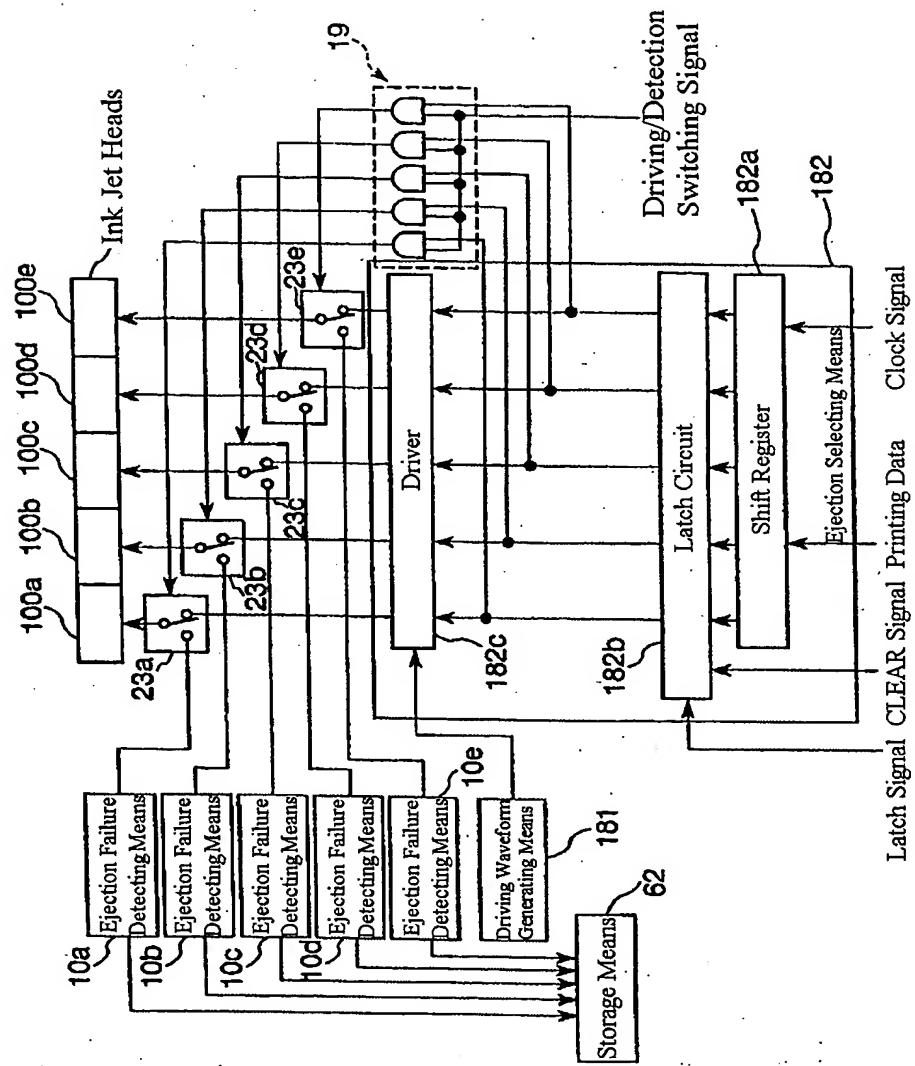


Fig. 29

29/46

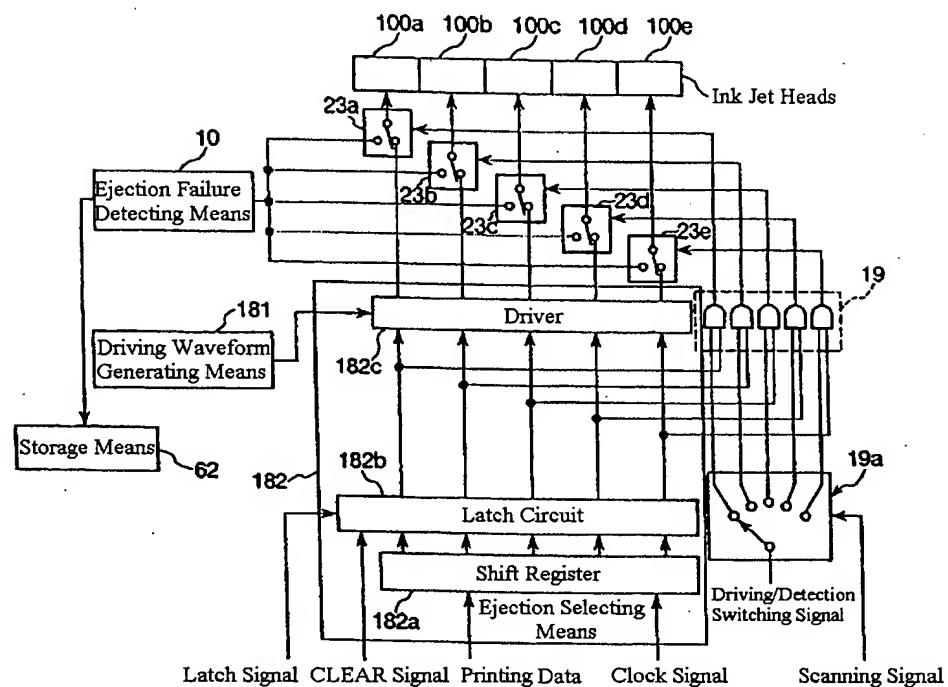


Fig. 30

30/46

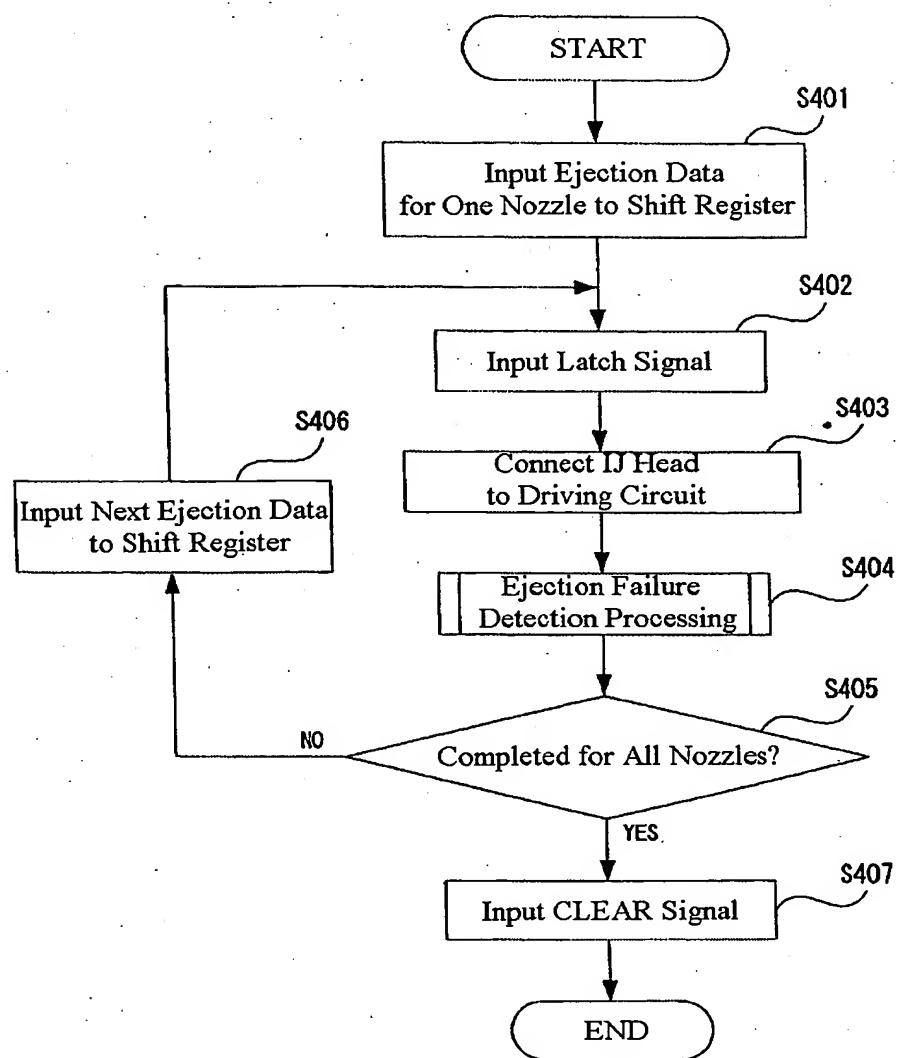


Fig. 31

31/46

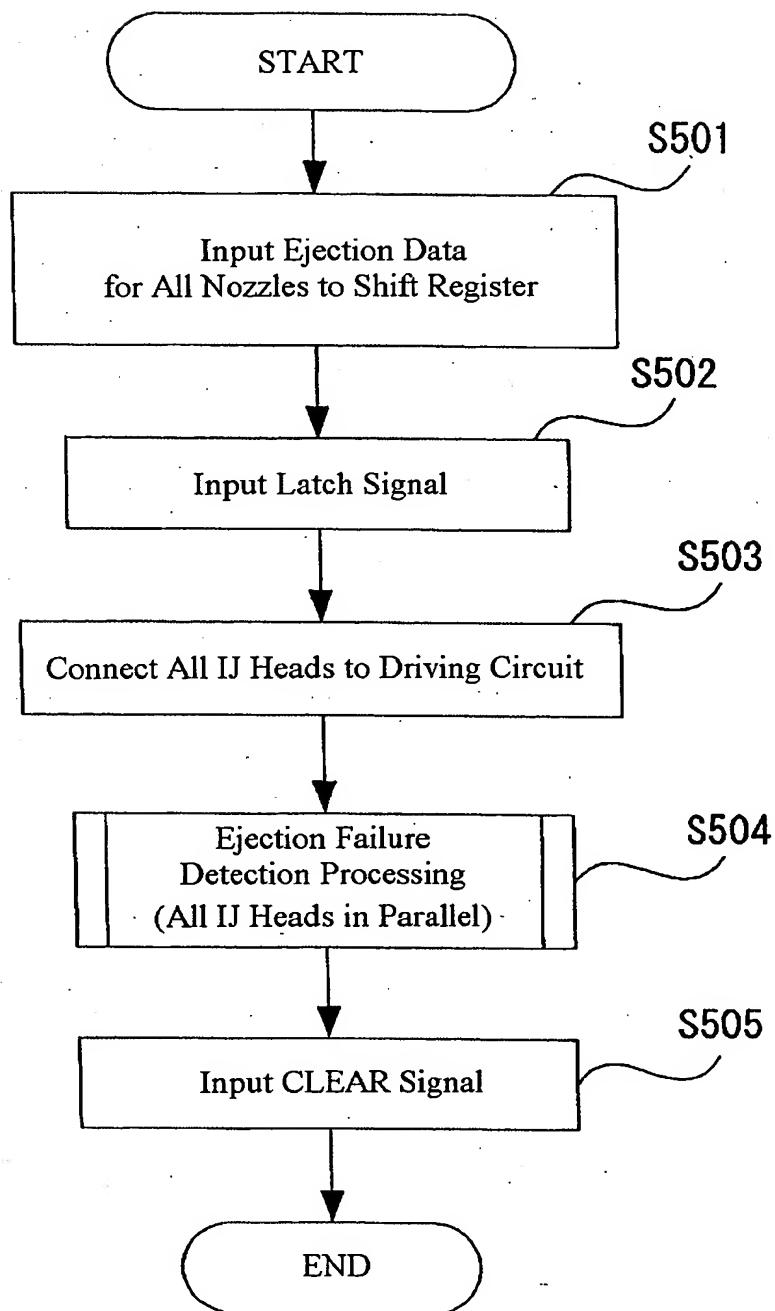


Fig. 32

32/46

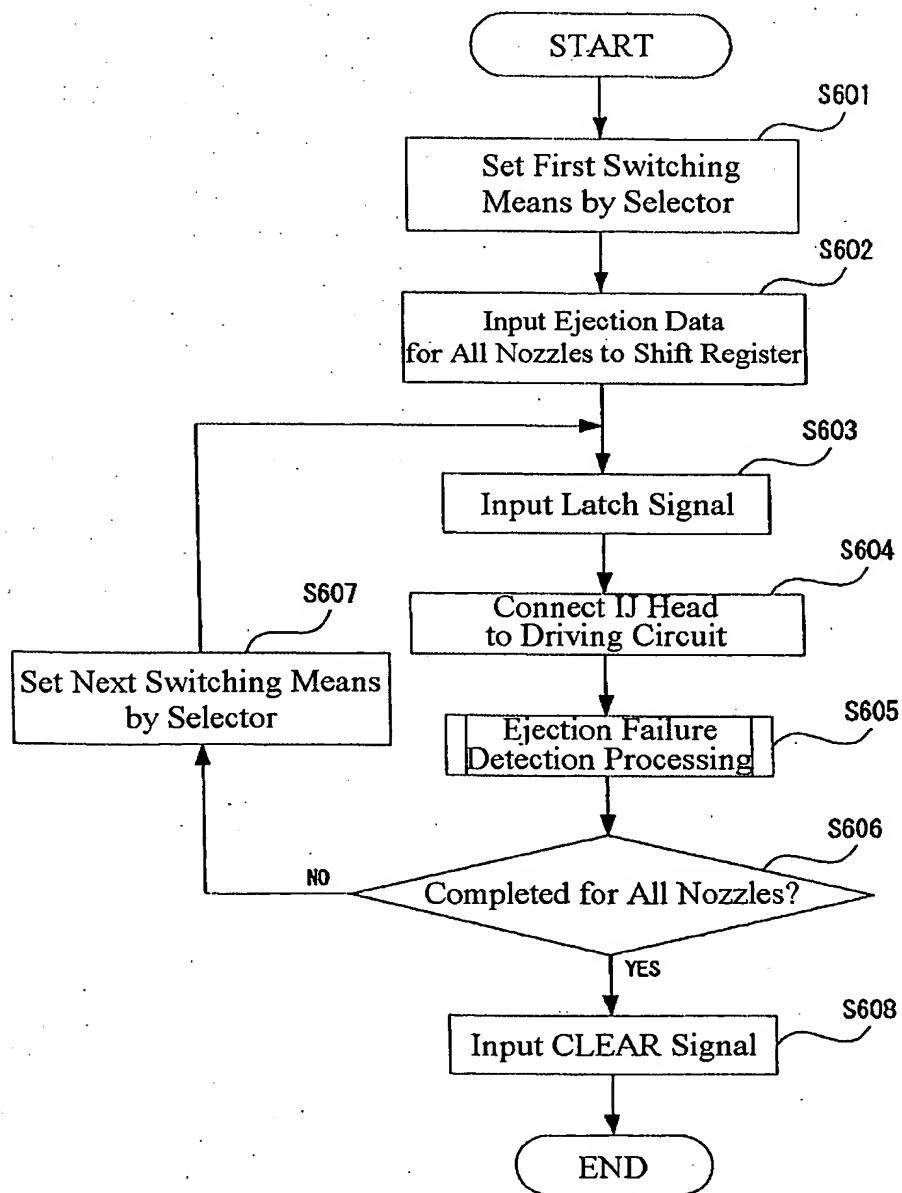


Fig. 33

33/46

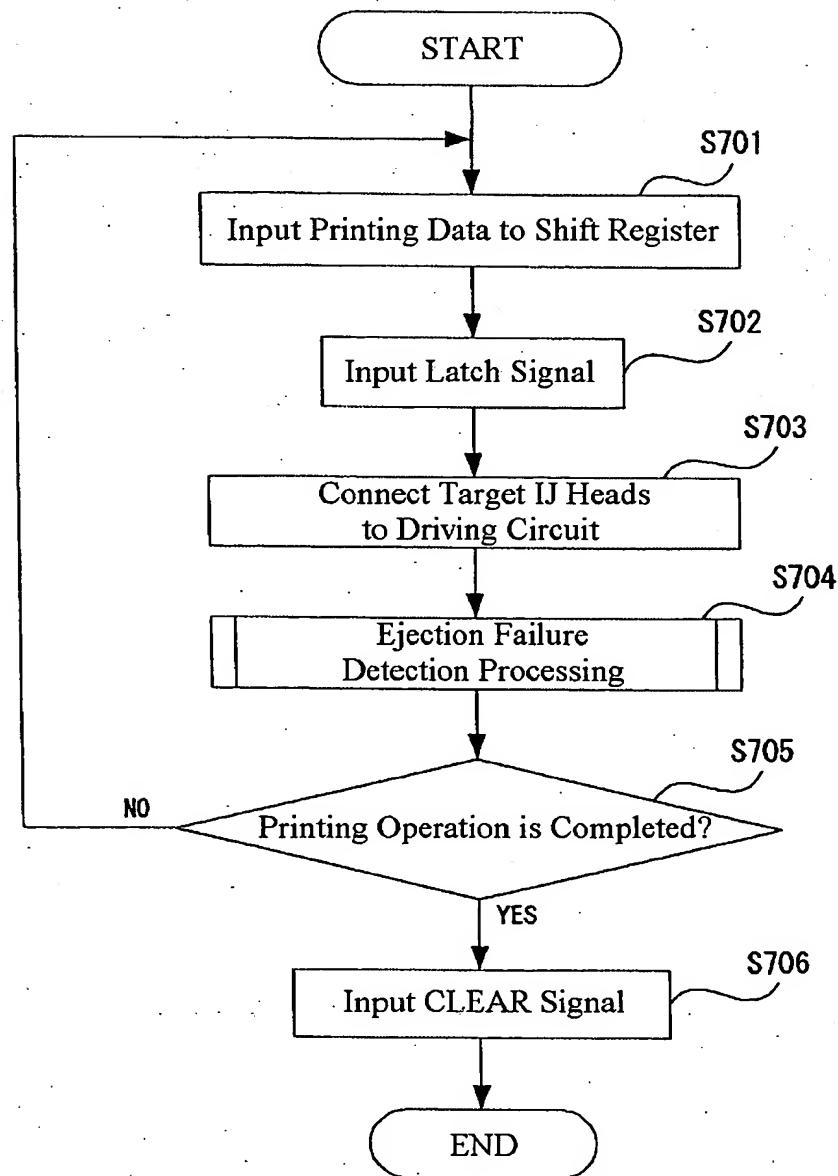


Fig. 34

34/46

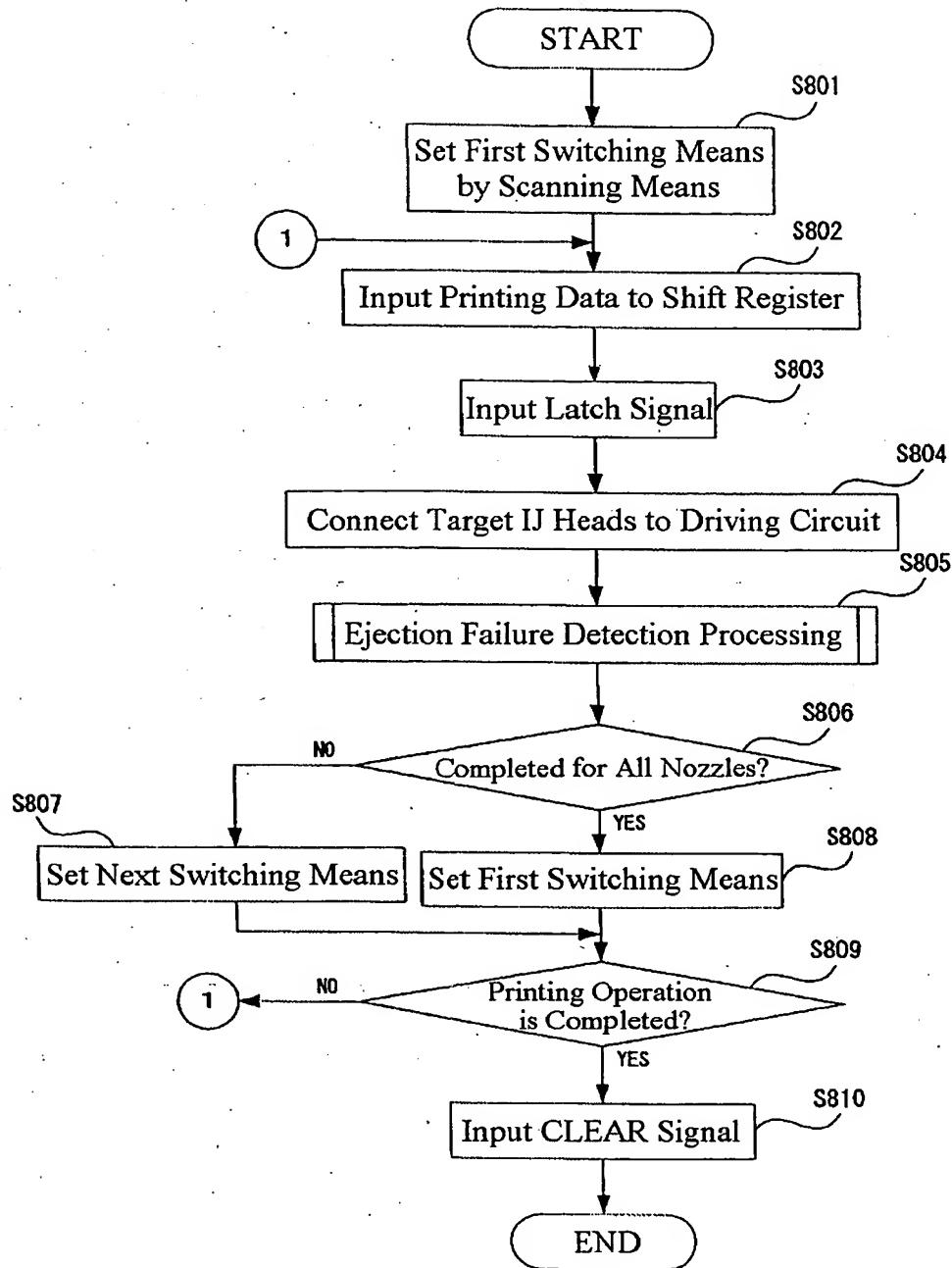


Fig. 35

35/46

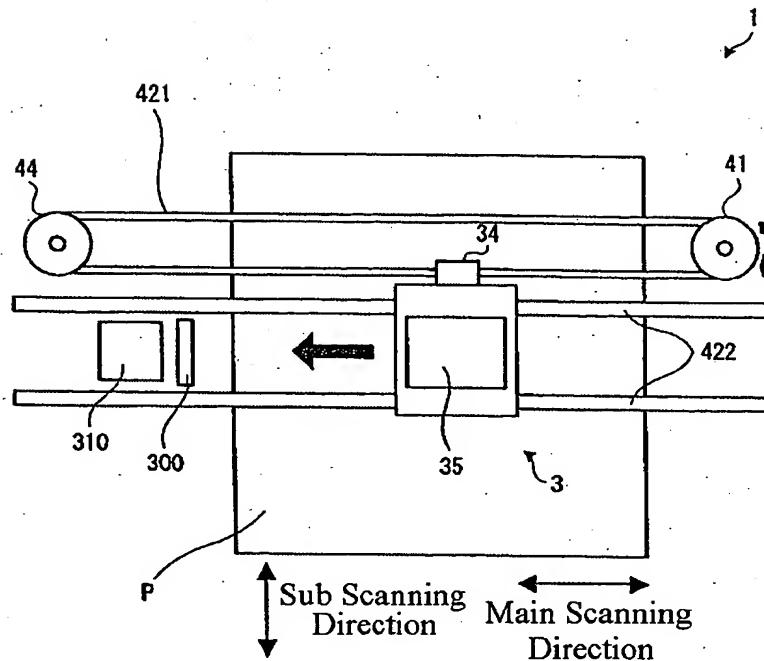


Fig. 36

36/46

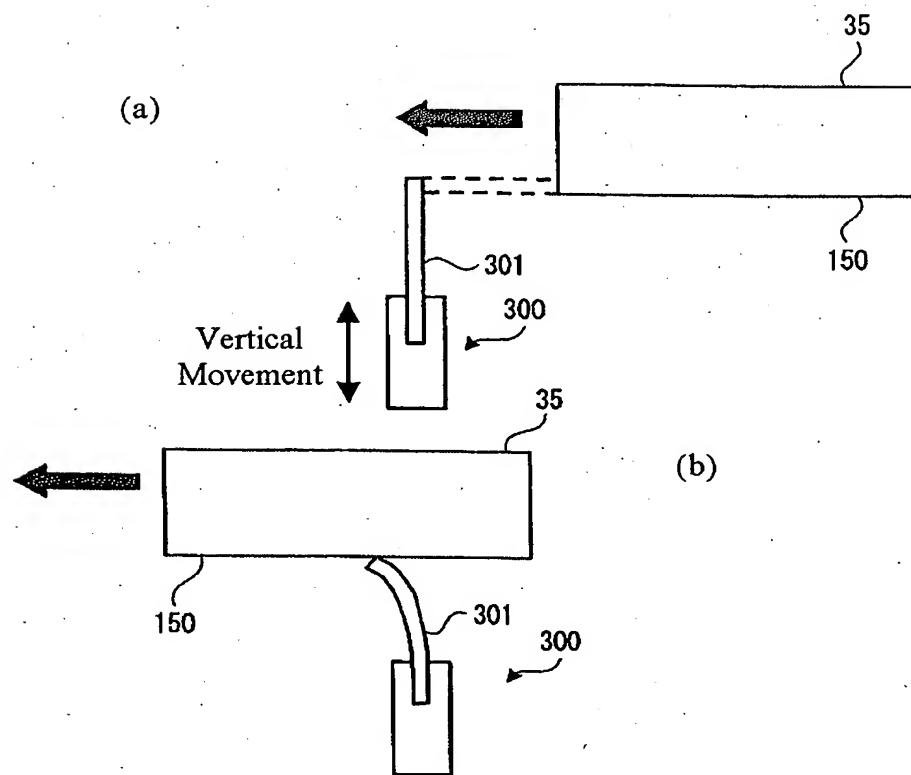


Fig. 37

37/46

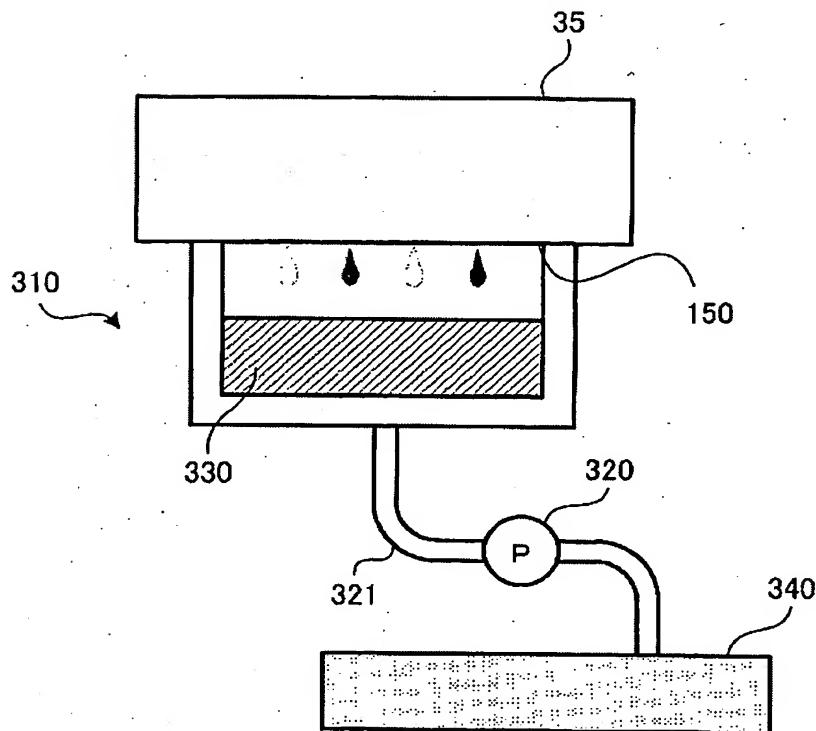


Fig. 38

38/46

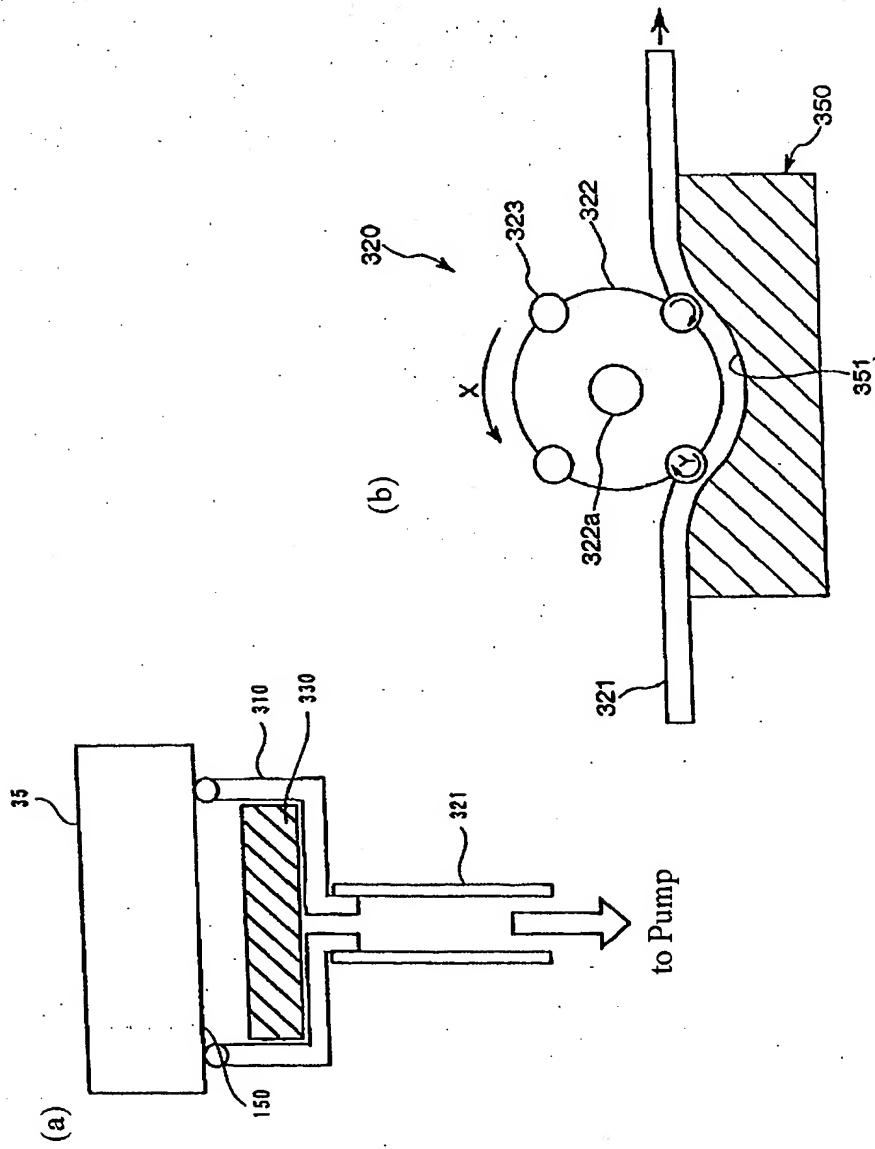


Fig. 39

39/46

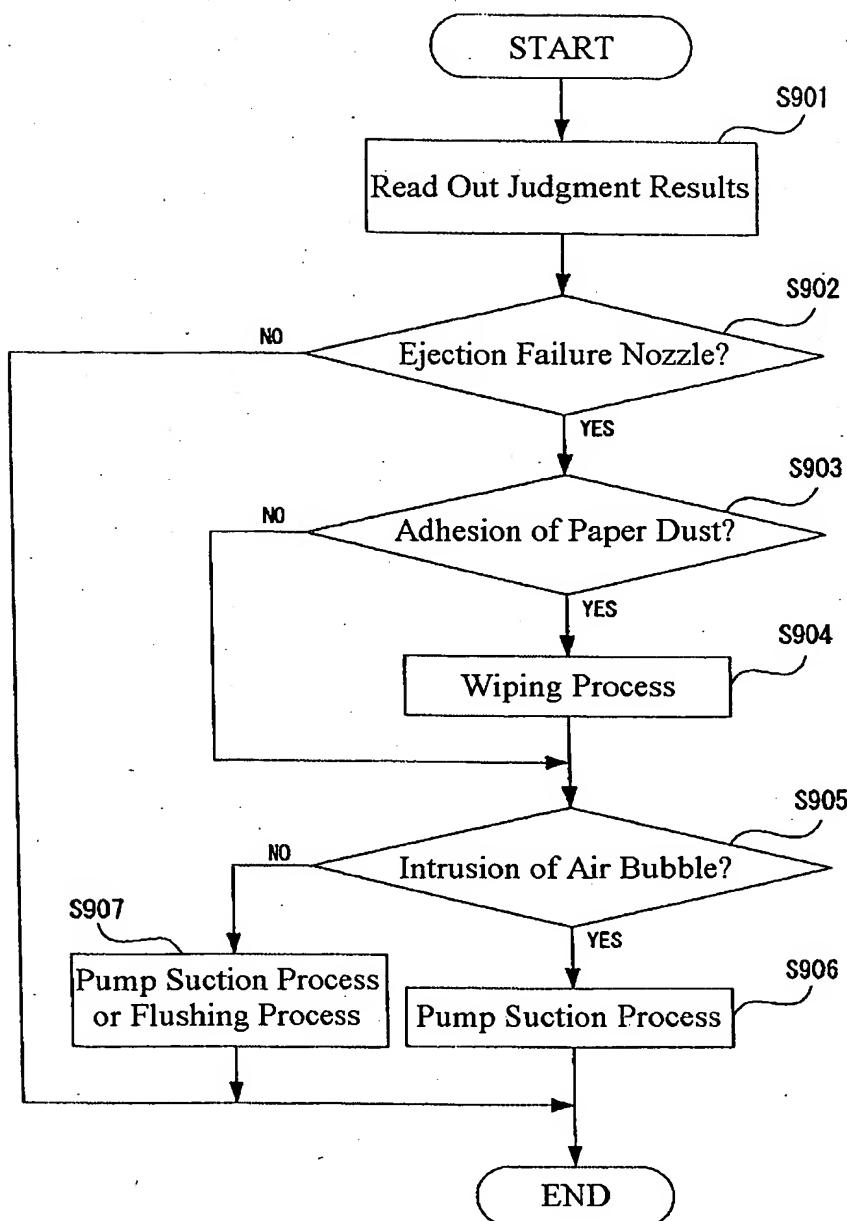


Fig. 40

40/46

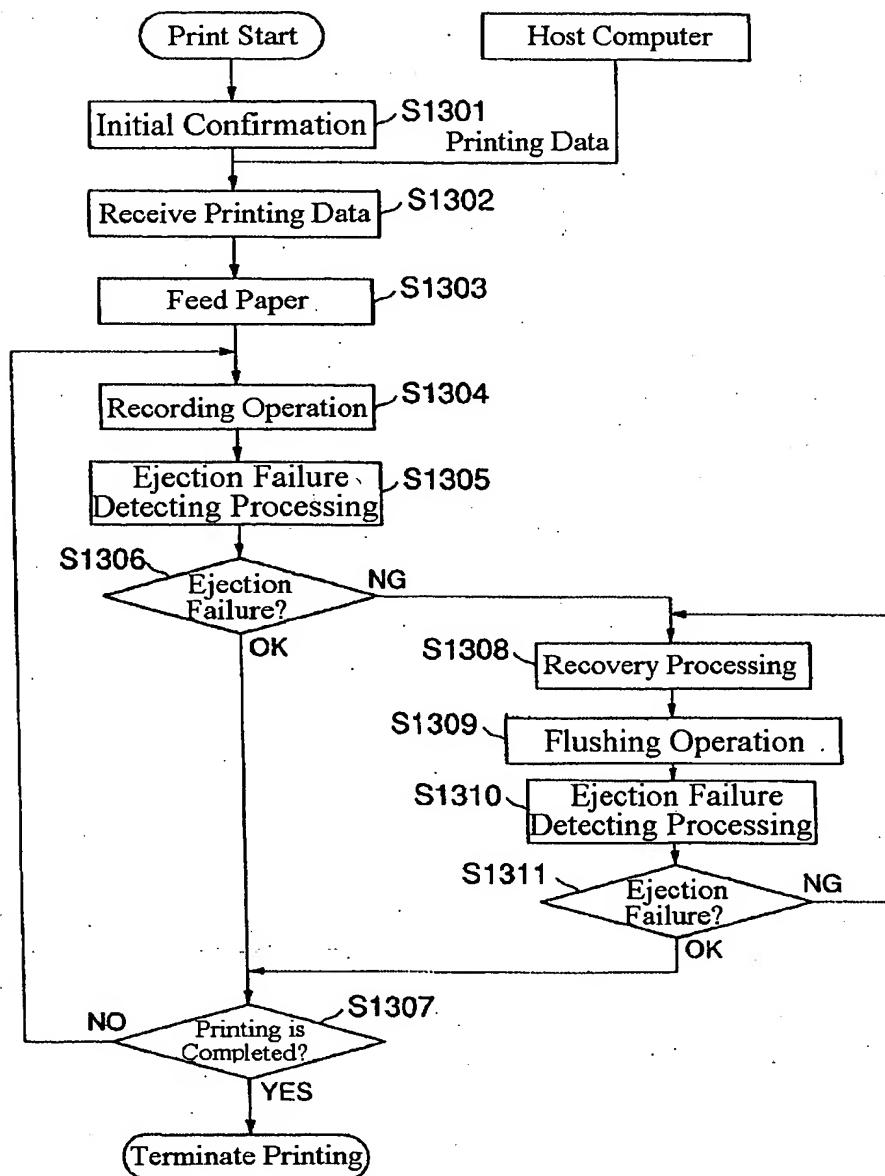


Fig. 41

41/46

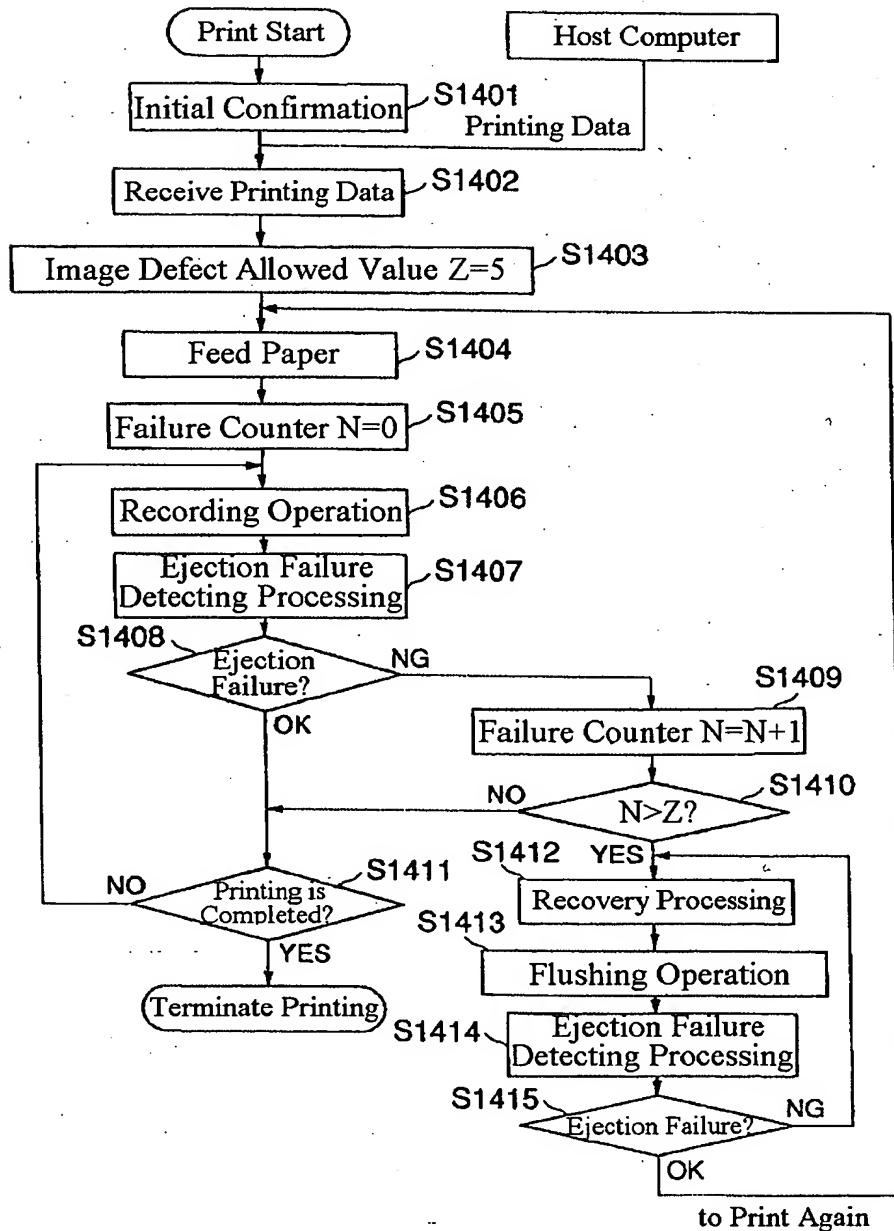


Fig. 42

42/46

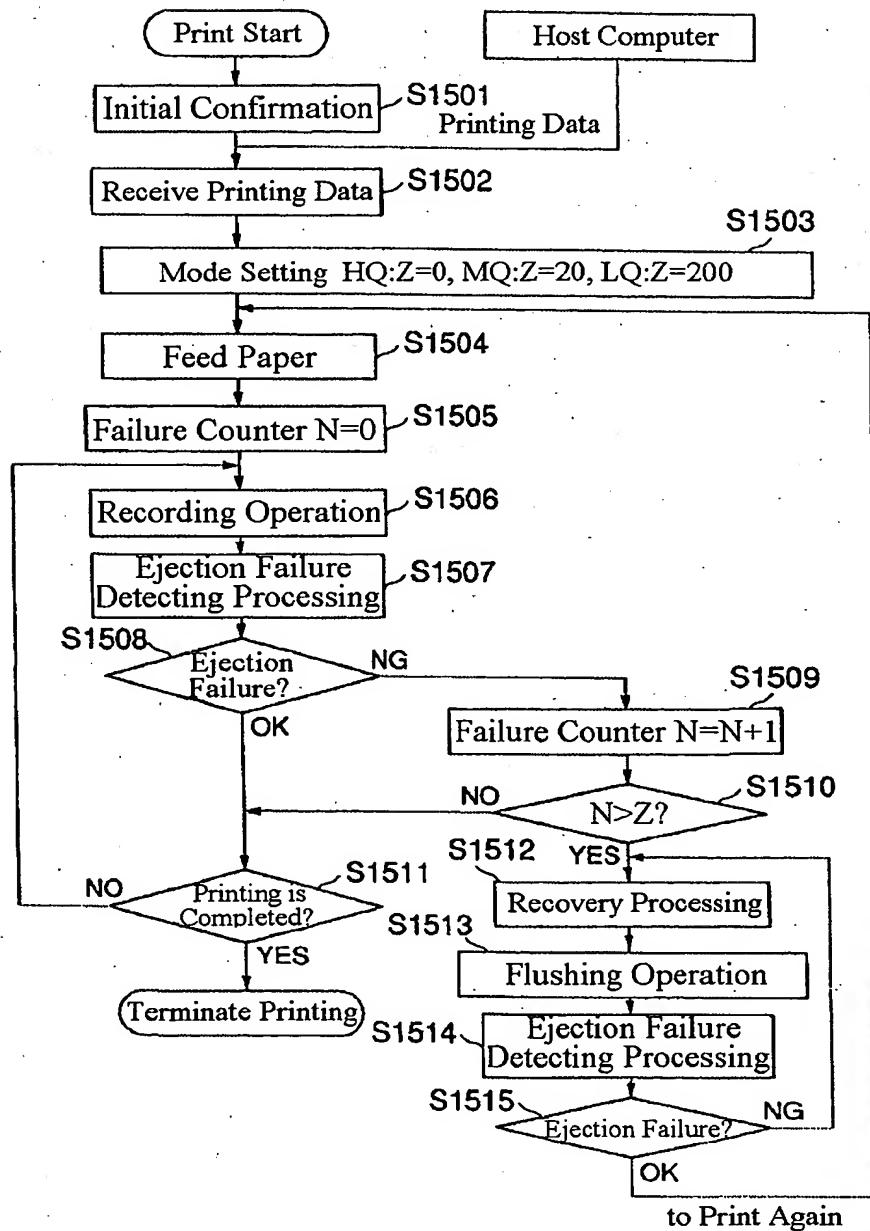


Fig. 43

43/46

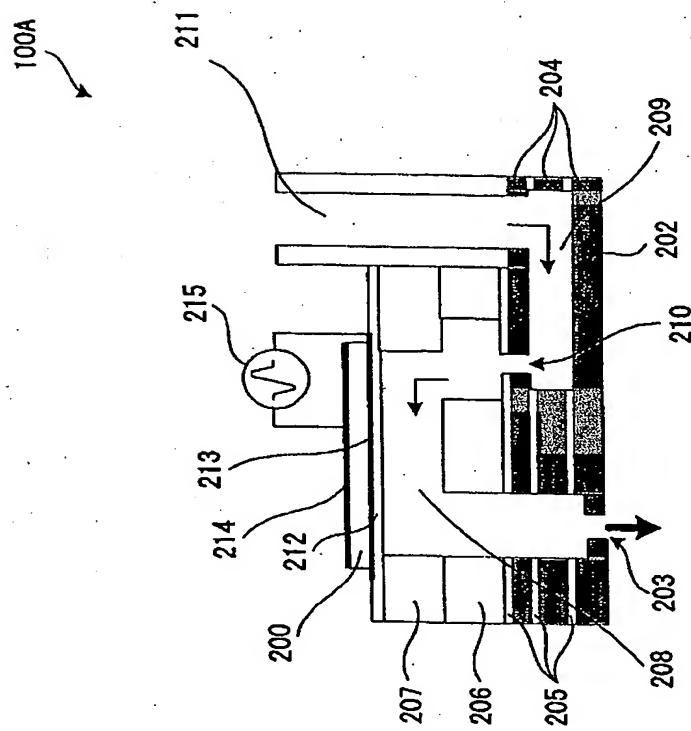


Fig. 44

44/46

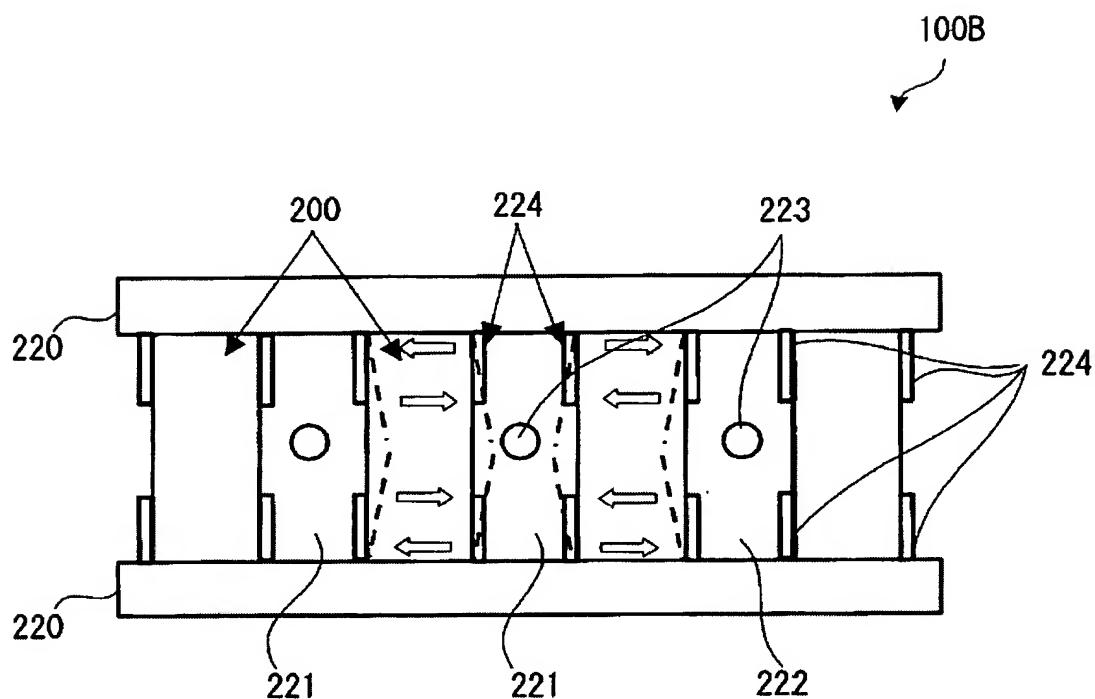


Fig. 45

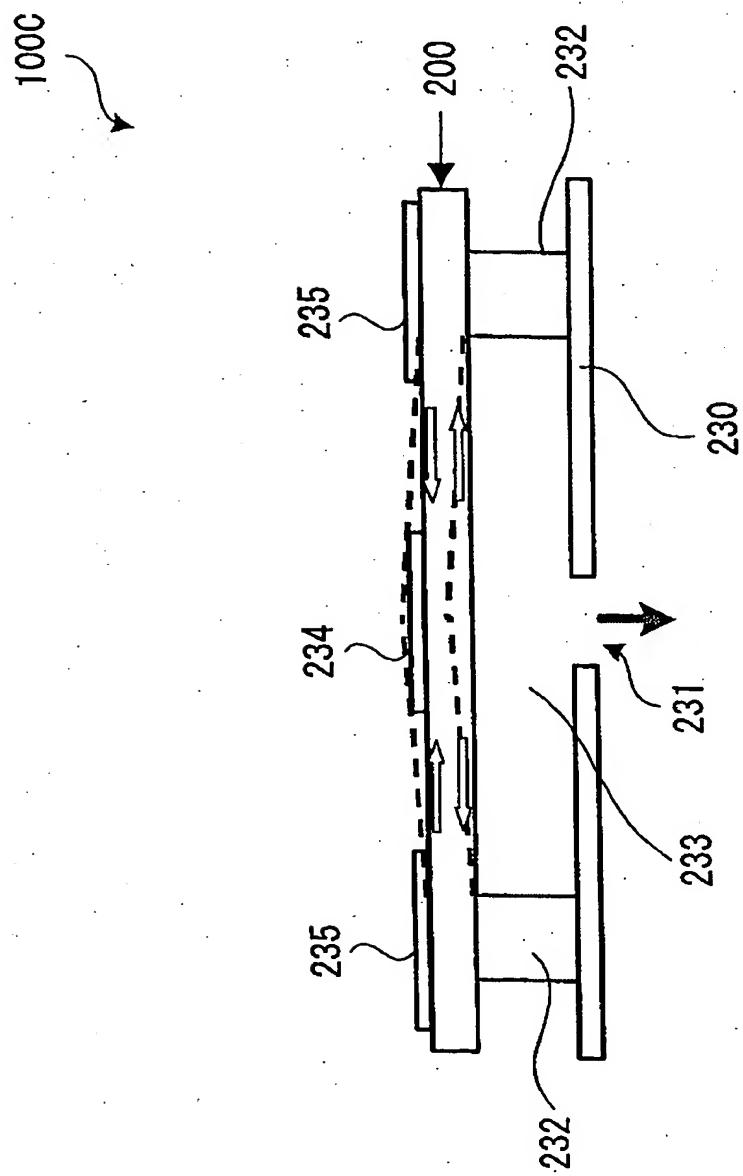


Fig. 46

46/46

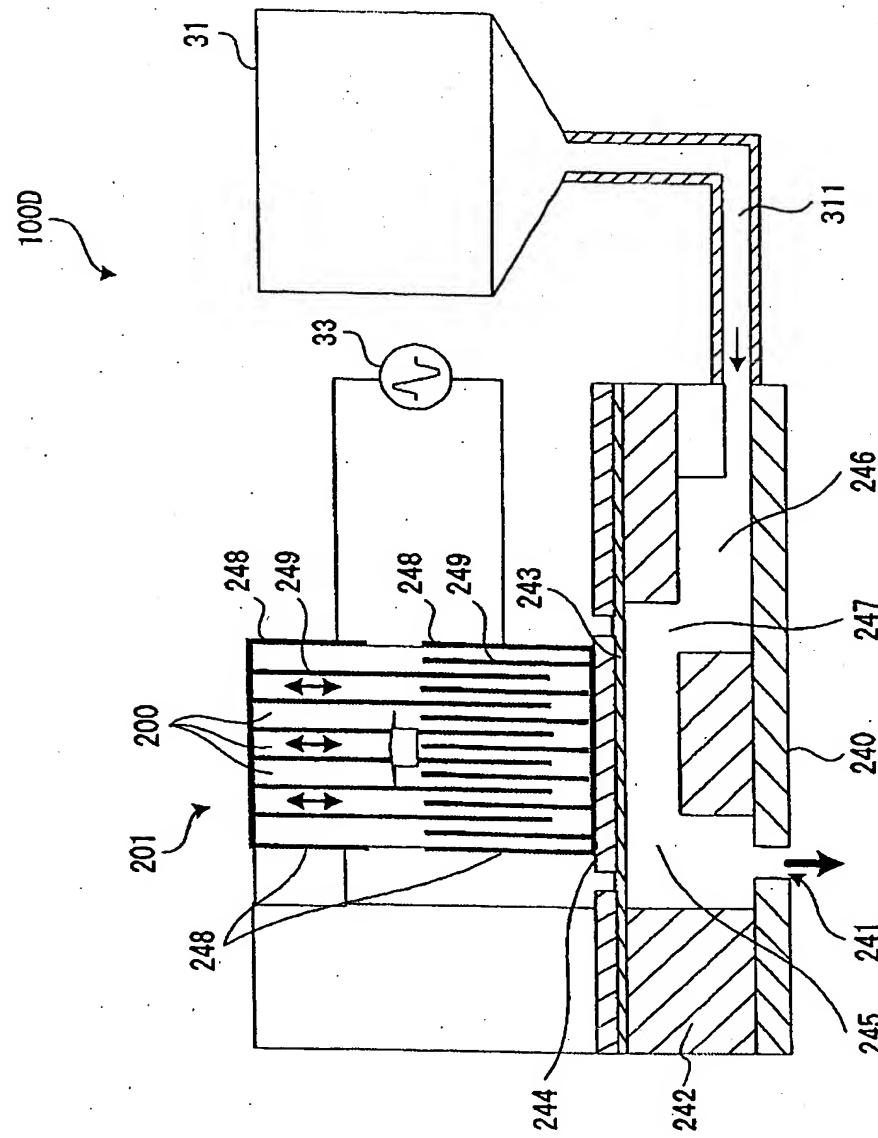


Fig. 47